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BREMEN-D

CPU : AMD Caspin
Chip Set : AMD RX881 + SB710
Remarks : Tigris Platform
Park-XT M2

Model Name : Bremen-D
PBA Name : MAIN
PCB Code : GCE :
NAN :
HAN :
Dev. Step : PV
Revision : 1.4
T.R. Date : 2009.11.10

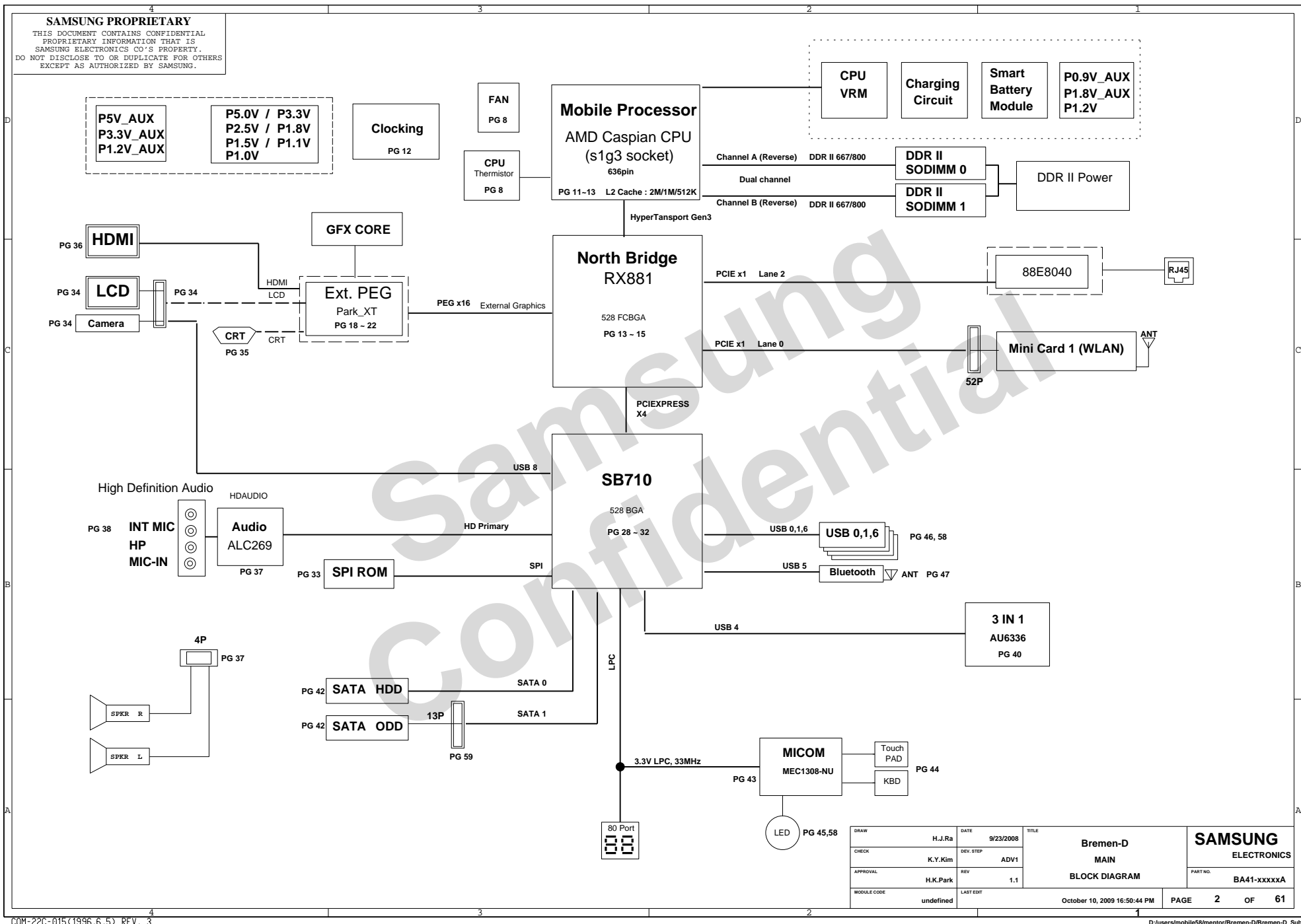
Design	CHECK	APPROVAL

Owner : SEC Mobile R & D Signature : X

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DRAW	XIE, BIN	DATE	10/10/2008	TITLE	Bremen-D	SAMSUNG
CHECK	GUO, LEI	DEV. STEP	PV	MAIN		ELECTRONICS
APPROVAL	LEE, BC	REV	1.0	COVER	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT	October, 28, 2009 11:35:37 AM	PAGE	1	OF



BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU_CORE	Core Voltage for CPU
EGFX_CORE	Core Voltage for GPU
P1.1V	VTT for RX881
P1.2V	Core Voltage for SB710, CPU_VDLT, RX881
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P1.0V	0.9V power rail for DDR (off in S3-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_STB	5.0V always power rail
P12.0V_ALW	12.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB710	Real Time Clock
Crystal	10MHz	MICOM	MEC1308-NU
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	88E8040
Crystal	25MHz	SATA	SB710

I²C / SMB Address

Devices	Address	Hex	Bus
S710	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 0010	D2h	Clock, Unused Clock Output Disable
Gfx (DTS)		41h	Gfx Thermal SMBUS Slave ID

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	NC
3	NC
4	3 IN 1
5	Bluetooth
6	SYSTEM PORT 2
7	NC
8	Camera
9	NC
10	NC

PCI Express Assign

PORT #	ASSIGNED TO
0	Mini Card (WLAN)
1	NC
2	LOM
3	NC
4	NC
5	NC

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0(strap0)
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REVISION HISTORY

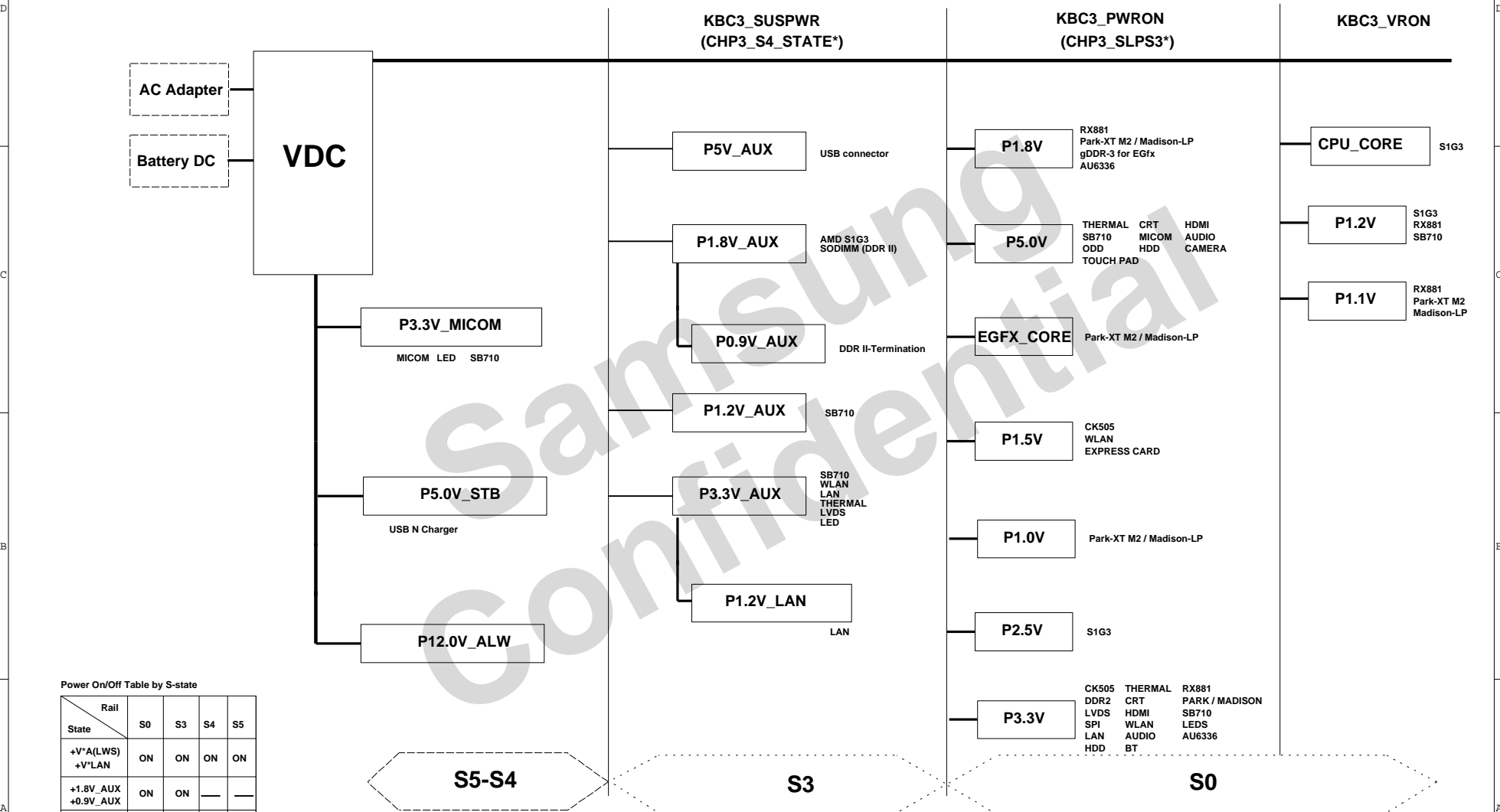
See rev notes for more information.

DRAW	H.J.Ra	DATE	08/18/2009	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1	MAIN	BOARD INFORMATION	ELECTRONICS
APPROVAL	H.K.Park	REV	1.1			PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	3	OF 61

POWER DIAGRAM

Rev 0.3

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Power On/Off Table by S-state

Rail State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V_AUX	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

S5-S4

S3

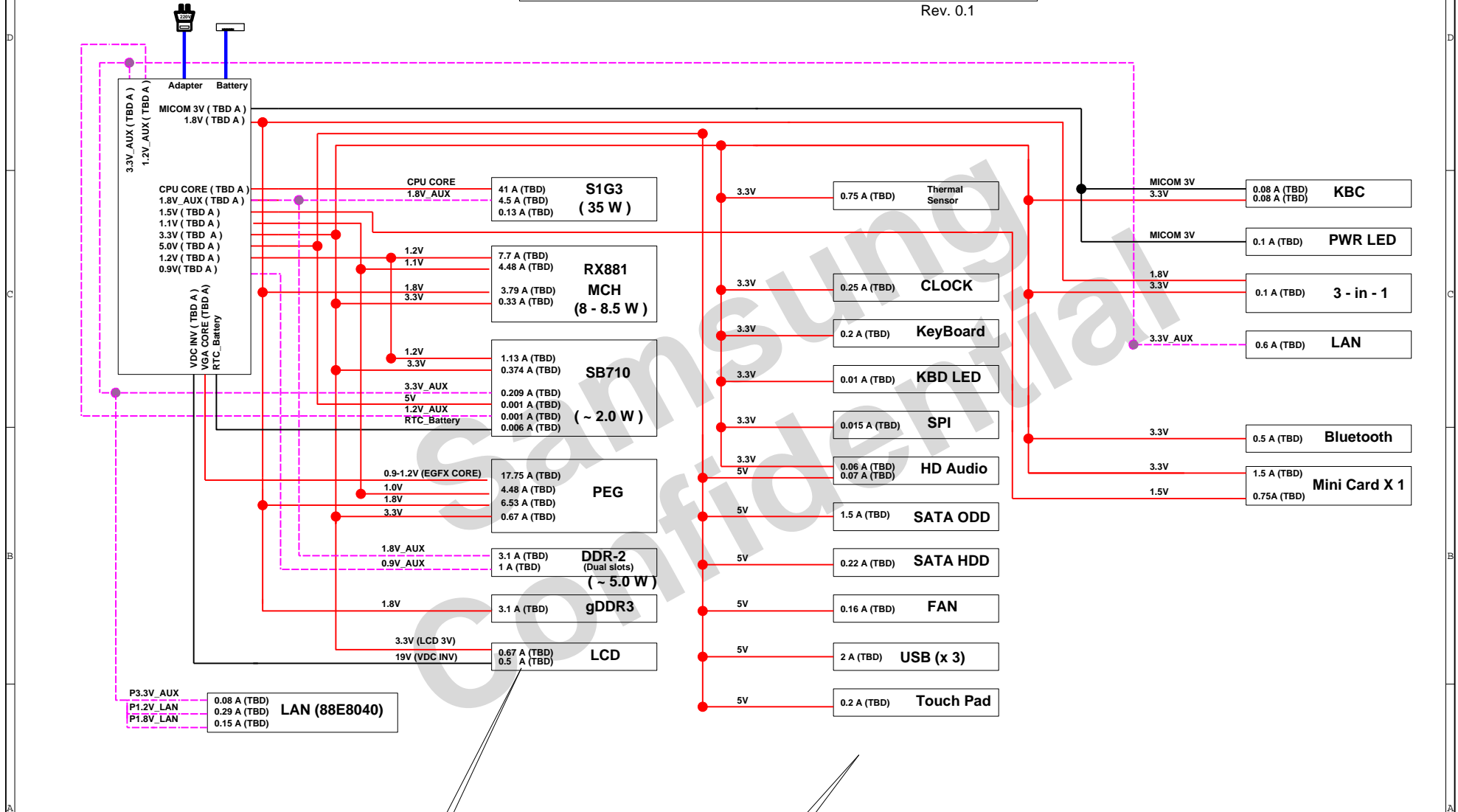
S0

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APPROVAL	H.K.Park	REV	1.1			
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POWER RAILS ANALYSIS

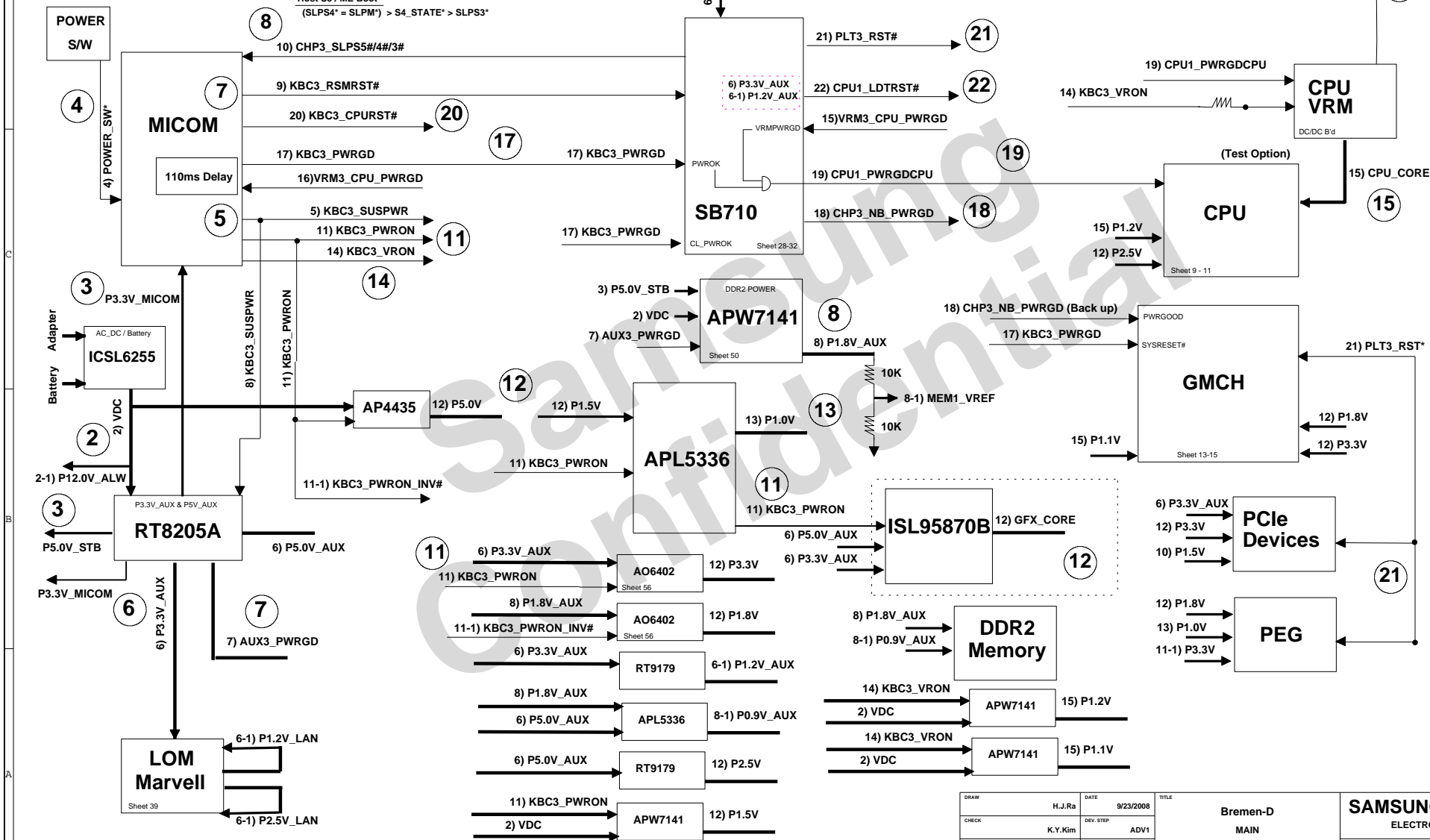
Rev. 0.1




Value by Datasheet/Application notes (Value by measurement)

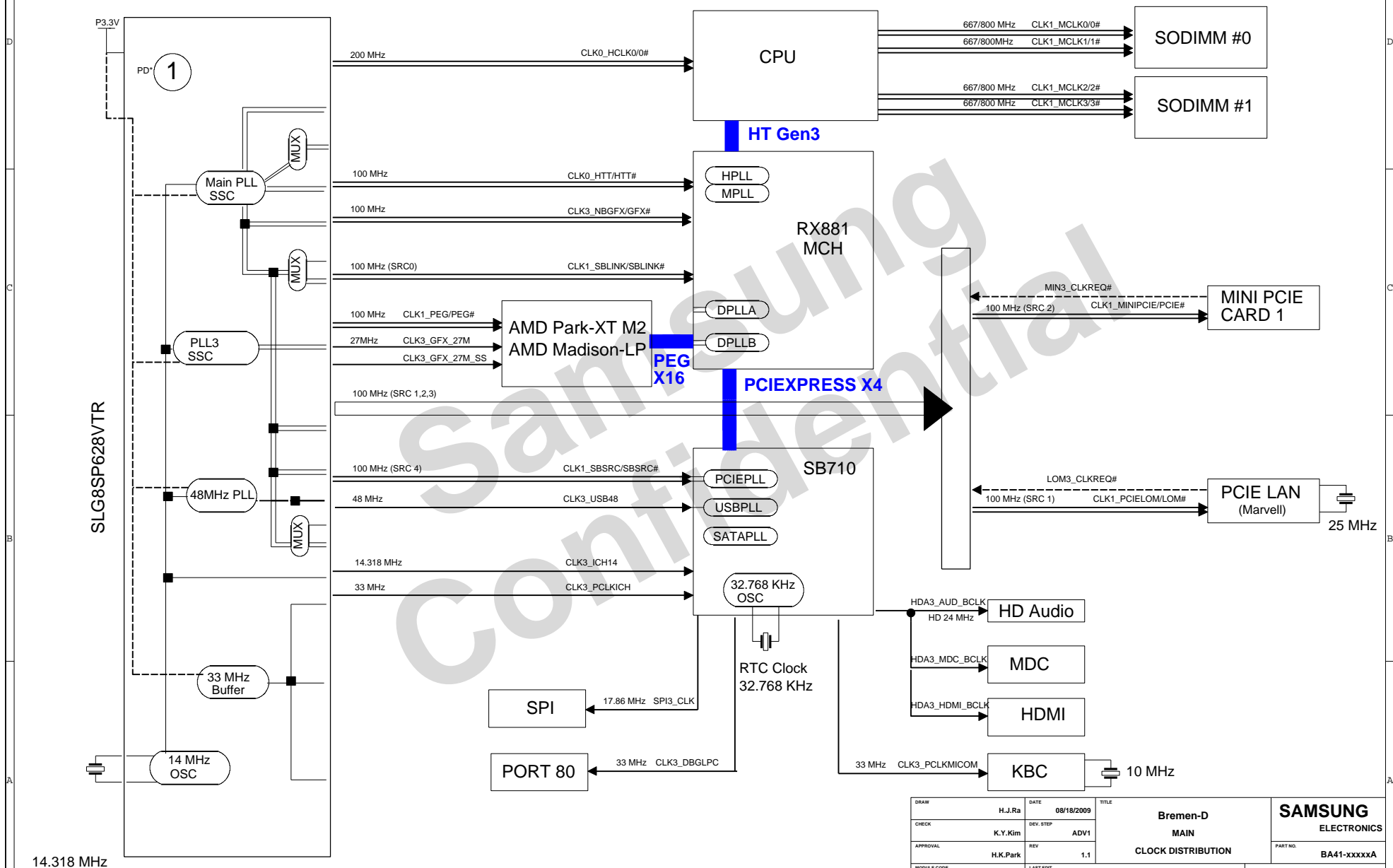
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APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	5	OF 61

M-2) KBC3 ME PWRON = 15) KBC3 PWRON

$$(SLPS4^* = SLPM^*) > S4 \text{ STATE}^* > SLPS3^*$$


DRAW	H.J.Ra	DATE	9/23/2008	Bremen-D MAIN POWER SEQUENCE			
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO.	
APPROVAL	H.K.Park	REV	1.1			BA41-xxxxxxA	
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE	6	OF 61

CLOCK DISTRIBUTION



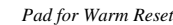
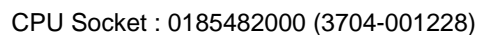
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[illegible]

SHDN_SEL MODE	
0	CH1(CPU MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

DESIGN	H.J.Ra	DATE	9/23/2008	Bremen-D THERMAL SENSOR THERMAL SENSOR EMC2112		SAMSUNG	
CHECK	K.Y.Kim	DEV. STEP	ADV1			ELECTRONICS	
APPROVAL	H.K.Park	REV	1.1			PART NO.	BA41-xxxxxxA
MODULE CODE	LAST EDIT			October 10, 2009 16:50:44 PM	PAGE	8	OF 61

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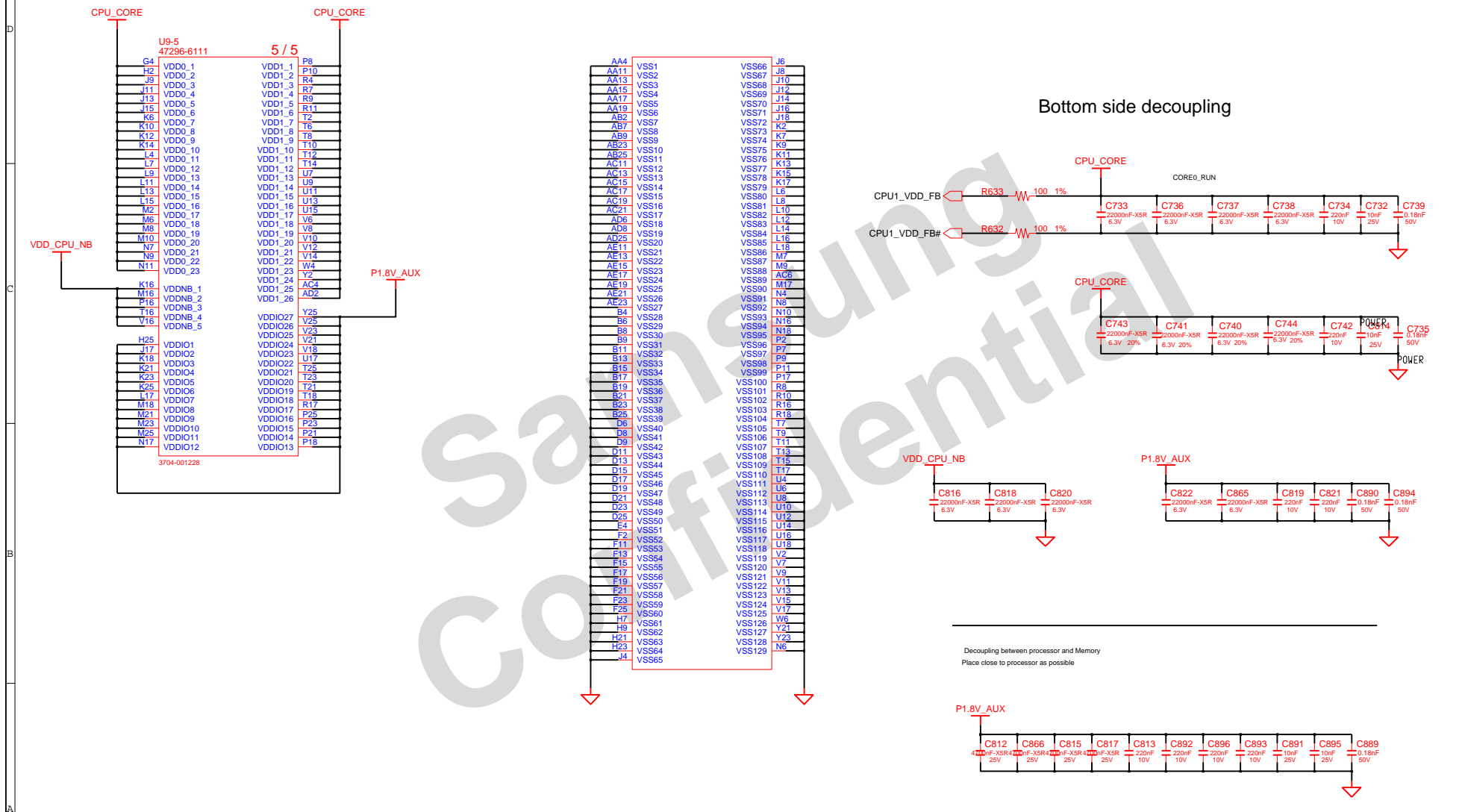


DRAW	H.J.Ra	DATE	9/23/2008	<p>Bremen-D</p> <p>CPU</p> <p>Caspian (1/3)</p>	<p>SAMSUNG</p> <p>ELECTRONICS</p>	
CHECK	K.Y.Kim	DEV. STEP	ADV1		PART NO.	BA41-xxxxxxA
APPROVAL	H.K.Park	REV	1.1			
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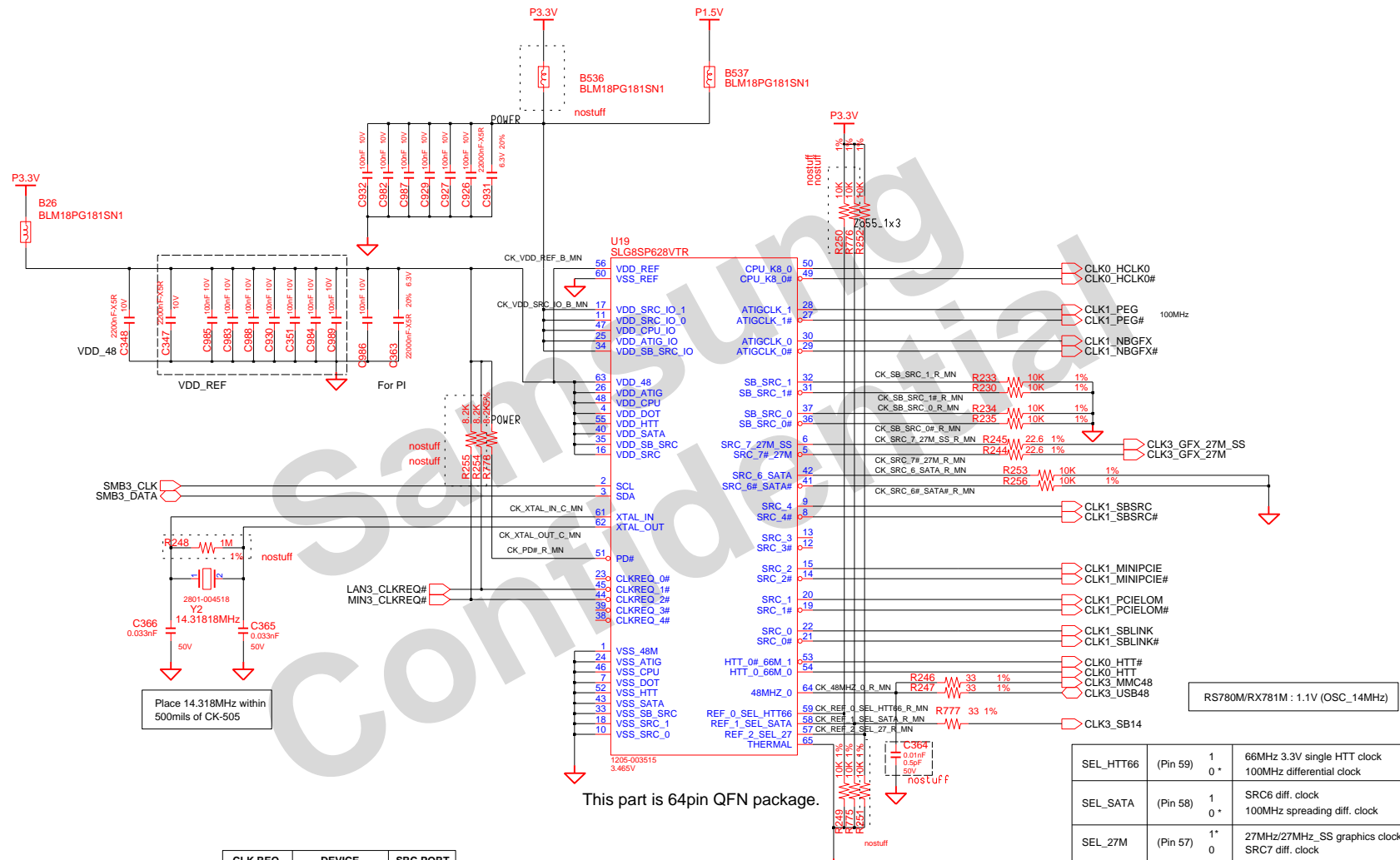
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APPROVAL	H.K.Park	REV	1.1								
PART NO.			BA41-xxxxxA								
MODULE CODE		undefined		LAST EDIT		October 10, 2009 16:50:44 PM		PAGE	10	OF	61

CPU_Caspian



DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D CPU Caspian (3/3)	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	11	OF 61

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This part is 64pin QFN package.

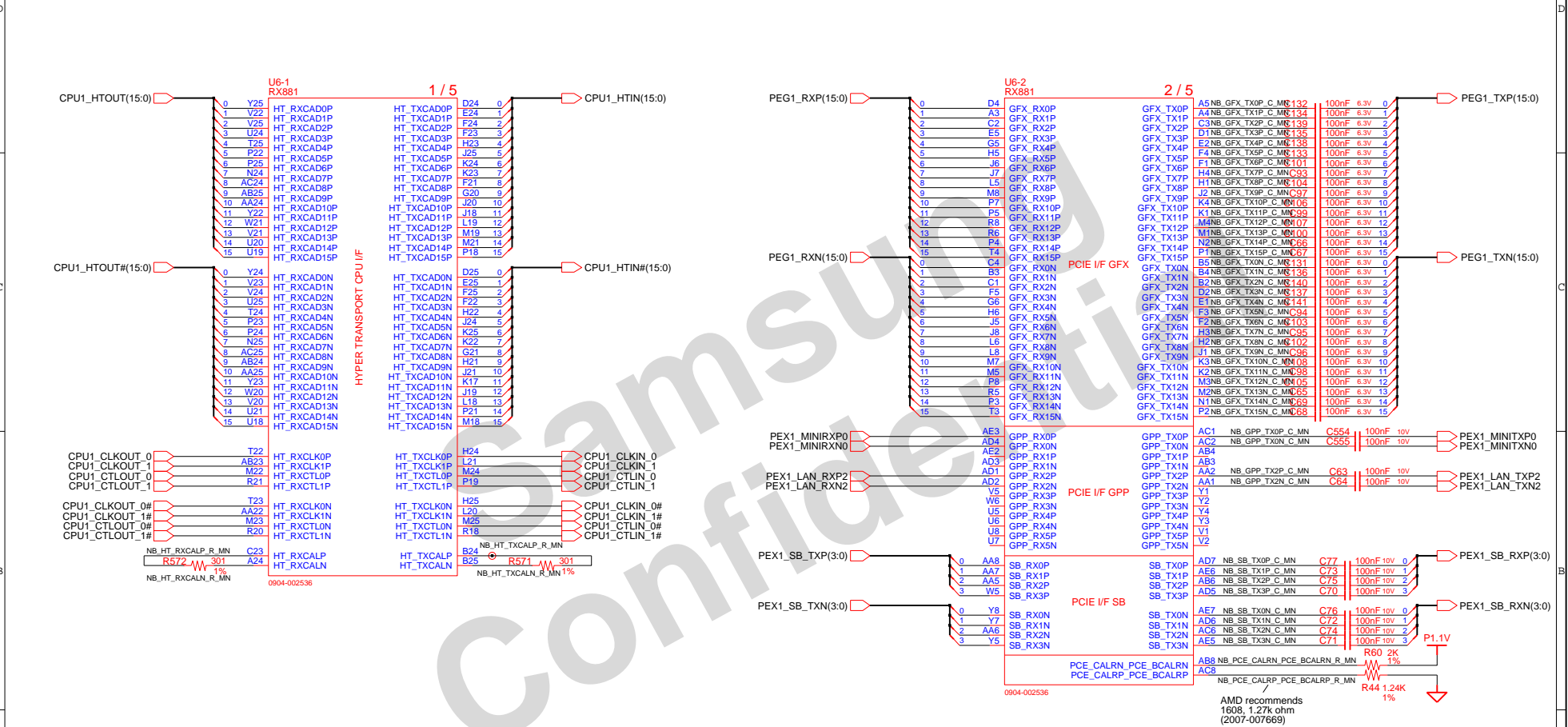
SEL_HTT66	(Pin 59)	1	66MHz 3.3V single HTT clock
		0 *	100MHz differential clock
SEL_SATA	(Pin 58)	1	SRC6 diff. clock
		0 *	100MHz spreading diff. clock
SEL_27M	(Pin 57)	1 *	27MHz/27MHz_SS graphics clock
		0	SRC7 diff. clock

DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1		MAIN_CLOCK_CIRCUIT
APPROVAL	H.K.Park	REV	1.1		CK_Clock_505M
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	12 OF 61

SAMSUNG
 ELECTRONICS
 PART NO. BA41-xxxxA

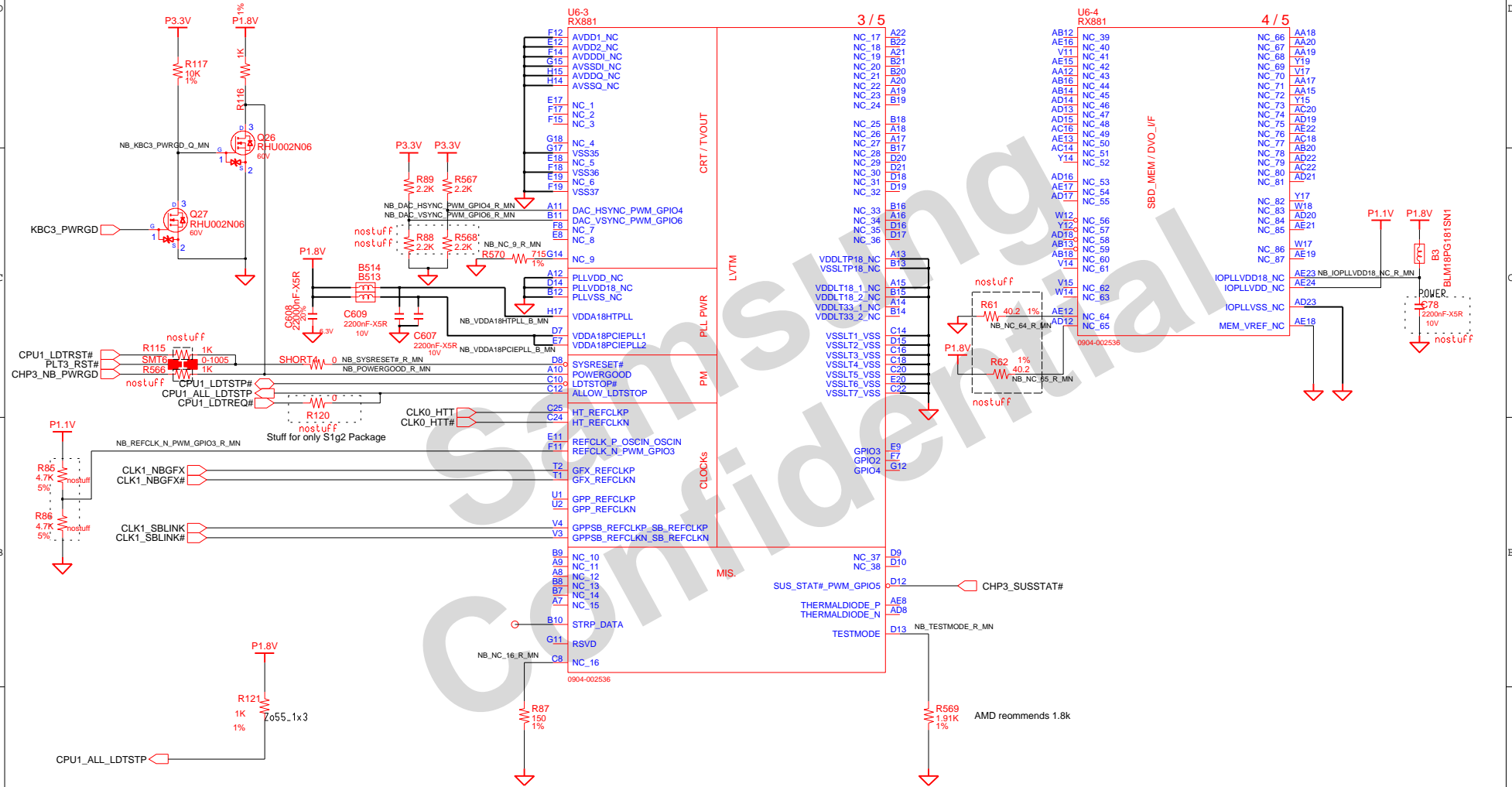
NB_RX881_AMD

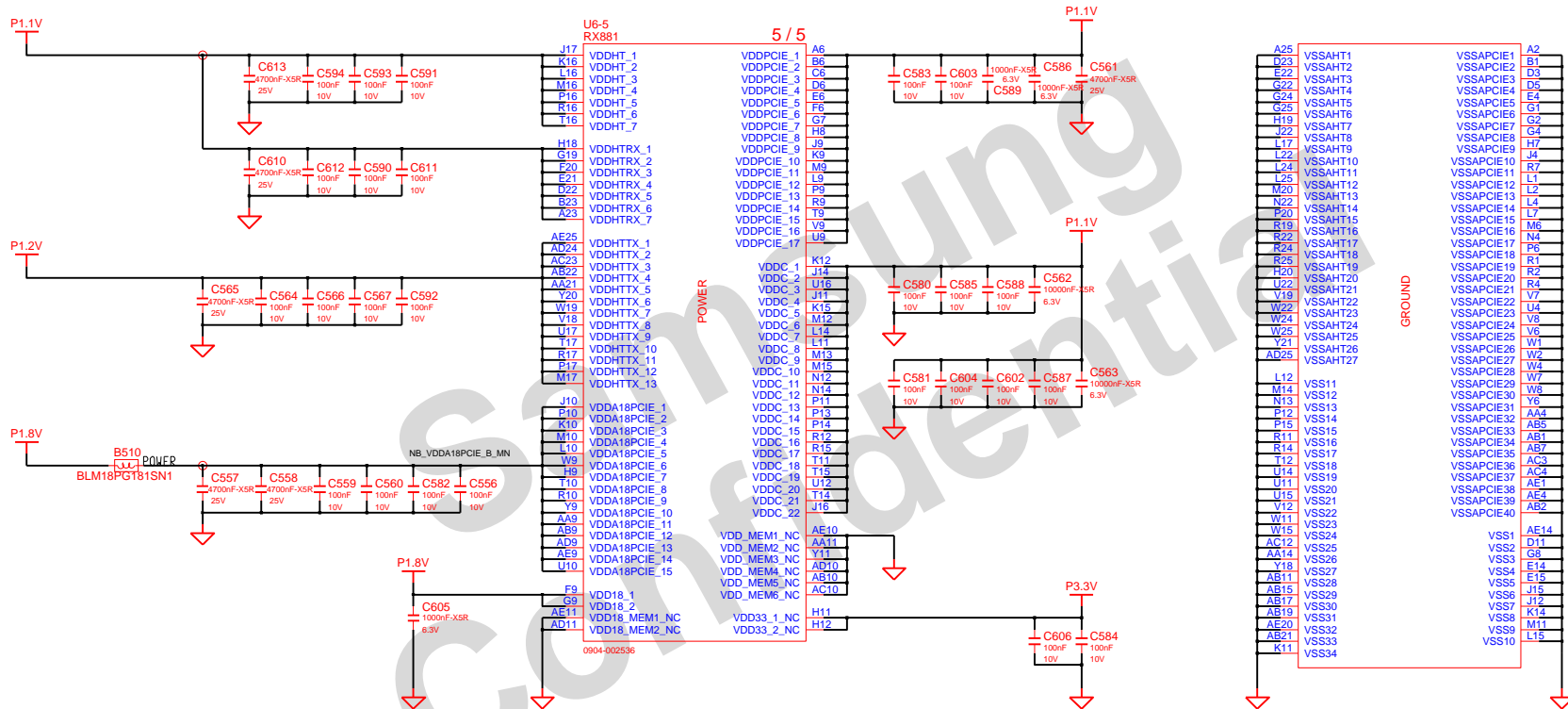
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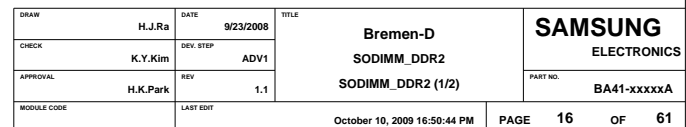
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CHECK	K.Y.Kim	DEV. STEP	ADV1		MCH_DDR2	ELECTRONICS
APPROVAL	H.K.Park	REV	1.1		RX881 (1/3)	PART NO.
MODULE CODE	undefined	LAST EDIT				BA41-xxxxxA
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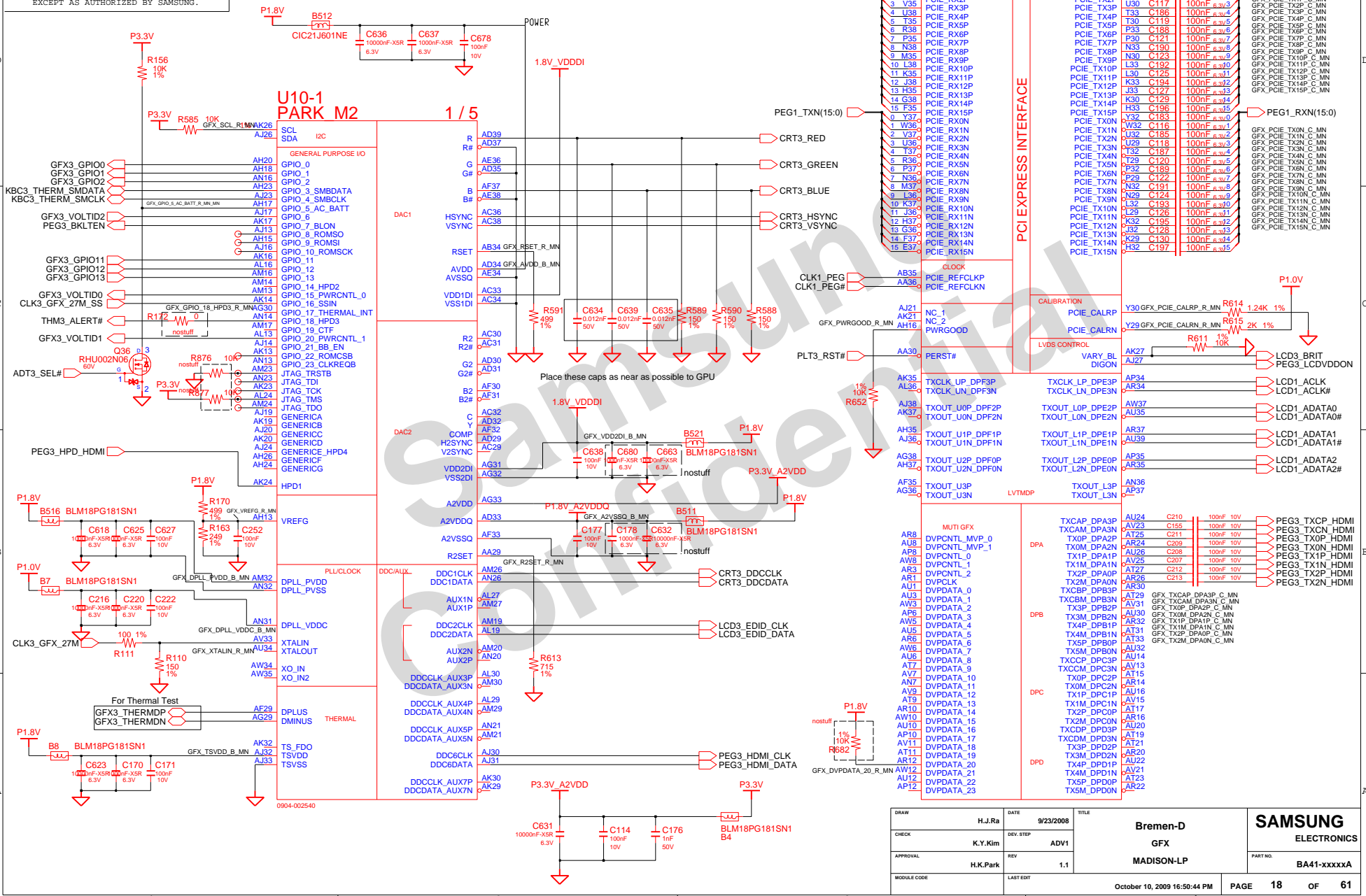


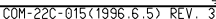


DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1	MCH_DDR2		
APPROVAL	H.K.Park	REV	1.1	RX881 (3/3)		
MODULE CODE		LAST EDIT				
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D:/users/mobile58/mentor/Bremen-D/Bremen-D_Sub

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COM-22C-015(1996.6.5) REV. 3

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U10-2
PARK M2 2 / 5

E39	PCIE_VSS_1	A3	GND_1
F34	PCIE_VSS_2	A37	GND_2
F39	PCIE_VSS_3	B7	GND_3
G33	PCIE_VSS_4	B9	GND_4
G34	PCIE_VSS_5	B11	GND_5
H31	PCIE_VSS_6	B13	GND_6
H34	PCIE_VSS_7	B15	GND_7
H39	PCIE_VSS_8	B17	GND_8
J31	PCIE_VSS_9	B19	GND_9
J34	PCIE_VSS_10	B21	GND_10
K31	PCIE_VSS_11	B23	GND_11
K34	PCIE_VSS_12	B25	GND_12
K39	PCIE_VSS_13	B27	GND_13
L31	PCIE_VSS_14	B29	GND_14
L34	PCIE_VSS_15	B31	GND_15
M34	PCIE_VSS_16	B33	GND_16
M39	PCIE_VSS_17	C1	GND_17
N31	PCIE_VSS_18	C39	GND_18
N34	PCIE_VSS_19	E5	GND_19
P31	PCIE_VSS_20	E35	GND_20
P34	PCIE_VSS_21	F7	GND_21
P39	PCIE_VSS_22	F9	GND_22
R34	PCIE_VSS_23	F11	GND_23
T31	PCIE_VSS_24	F13	GND_24
T34	PCIE_VSS_25	F15	GND_25
T39	PCIE_VSS_26	F17	GND_26
U31	PCIE_VSS_27	F19	GND_27
U34	PCIE_VSS_28	F21	GND_28
Y34	PCIE_VSS_29	F23	GND_29
Y39	PCIE_VSS_30	F25	GND_30
W31	PCIE_VSS_31	F27	GND_31
W34	PCIE_VSS_32	F29	GND_32
Y34	PCIE_VSS_33	F31	GND_33
Y39	PCIE_VSS_34	F33	GND_34
AB39	PCIE_VSS_35	G2	GND_35
		G6	GND_36
		H9	GND_37
		J2	GND_38
		J6	GND_39
		J8	GND_40
		J27	GND_41
		K7	GND_42
		K14	GND_43
		L2	GND_44
		L6	GND_45
		L11	GND_46
		L17	GND_47
		L22	GND_48
		L24	GND_49
		M17	GND_50
		M22	GND_51
		M24	GND_52
		N2	GND_53
		N6	GND_54
		N16	GND_55
		N18	GND_56
		N21	GND_57
		N23	GND_58
		N25	GND_59
		R2	GND_60

GND

0904-002540

AC21	GND_120	R6	GND_61
AC23	GND_121	R15	GND_62
AC26	GND_122	R17	GND_63
AC28	GND_123	R20	GND_64
AD9	GND_124	R22	GND_65
AD15	GND_125	R24	GND_66
AD17	GND_126	R27	GND_67
AD20	GND_127	T11	GND_68
AD22	GND_128	T13	GND_69
AD24	GND_129	T16	GND_70
AE2	GND_130	T18	GND_71
AE6	GND_131	T21	GND_72
AF10	GND_132	T23	GND_73
AF18	GND_133	T26	GND_74
AF21	GND_134	U2	GND_75
AG2	GND_135	U6	GND_76
AG5	GND_136	U13	GND_77
AG9	GND_137	U15	GND_78
AG17	GND_138	U17	GND_79
AG20	GND_139	U20	GND_80
AG22	GND_140	U22	GND_81
AG27	GND_141	U24	GND_82
AJ2	GND_142	U27	GND_83
AJ6	GND_143	V11	GND_84
AJ8	GND_144	V13	GND_85
AJ10	GND_145	V16	GND_86
AJ11	GND_146	V18	GND_87
AJ28	GND_147	V21	GND_88
AK7	GND_148	V23	GND_89
AK11	GND_149	V26	GND_90
AL2	GND_150	W2	GND_91
AL5	GND_151	W6	GND_92
AL8	GND_152	Y15	GND_93
AL11	GND_153	Y17	GND_94
AL14	GND_154	Y20	GND_95
AL17	GND_155	Y22	GND_96
AL20	GND_156	Y24	GND_97
AR5	GND_157	Y27	GND_98
AL23	GND_158	AA2	GND_99
AL26	GND_159	AA6	GND_100
AL32	GND_160		
AM9	GND_161		
AM11	GND_162		
AM17	GND_163		
AM2	GND_164		
AN2	GND_165		
AN6	GND_166		
AN8	GND_167		
AN30	GND_168		
AP7	GND_169		
AP9	GND_170		
AP11	GND_171		
AL21	GND_172		
	GND_173		
	GND_174		

GND

VSS_MECH_1
VSS_MECH_2
VSS_MECH_3

A39
AW1
AW39

DESIGN	H.J.Ra	DATE	9/3/2009	TITLE	Bremen-D GFX MADISON-LP	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	22	OF 61

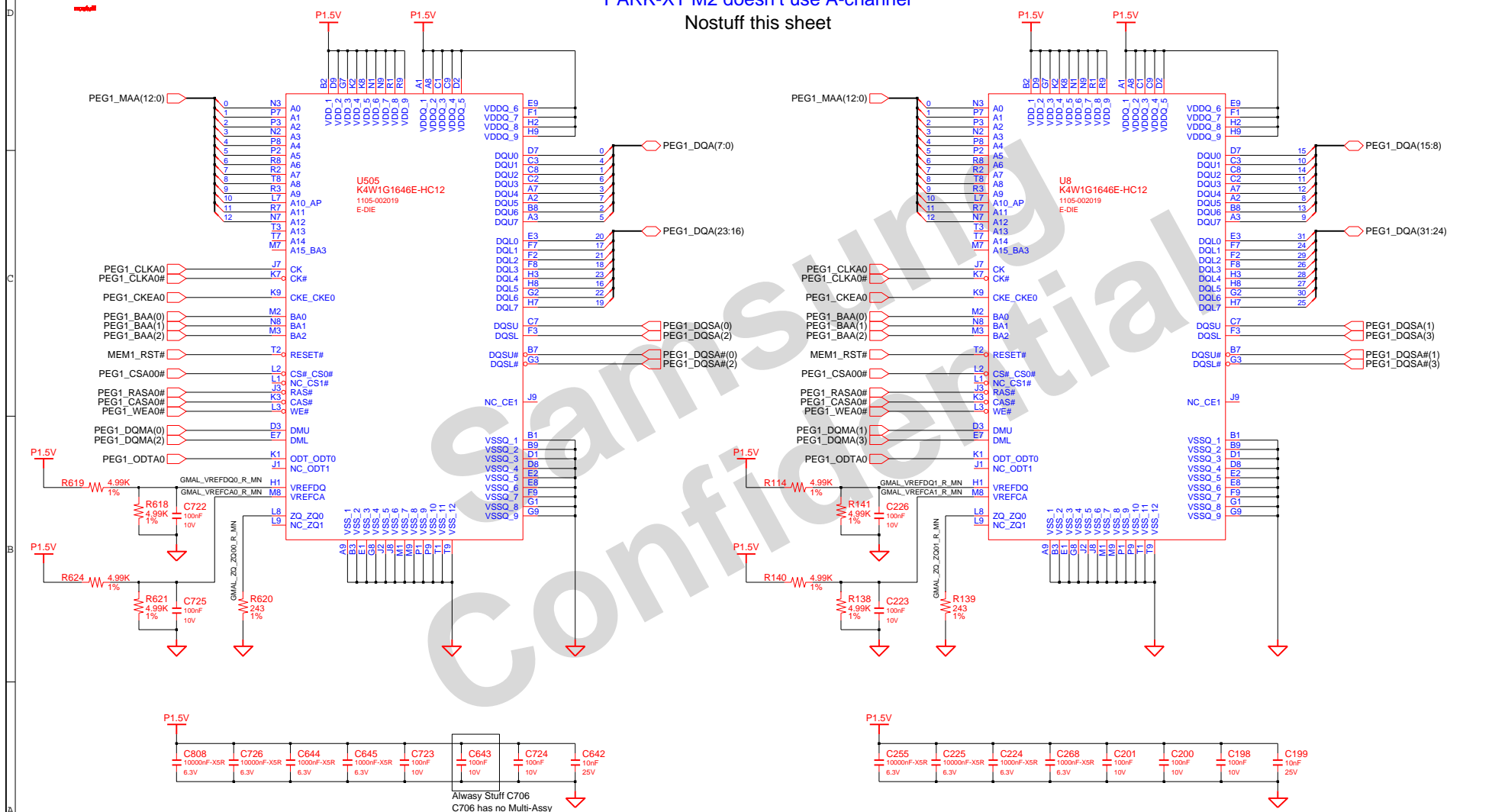
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A-channel Lower Data

PARK-XT M2 doesn't use A-channel

Nostuff this sheet



PEG1_CLKA0# \rightarrow R622 \rightarrow POWER \rightarrow C727 \rightarrow 10nF 25V
PEG1_CLKA0# \rightarrow R623 \rightarrow 56 1% \rightarrow C727 \rightarrow 10nF 25V

DESIGN	H.J.Ra	DATE	9/3/2009	TITLE	Bremen-D GRAPHICS MEMORY gDDR3	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	23 OF 61	

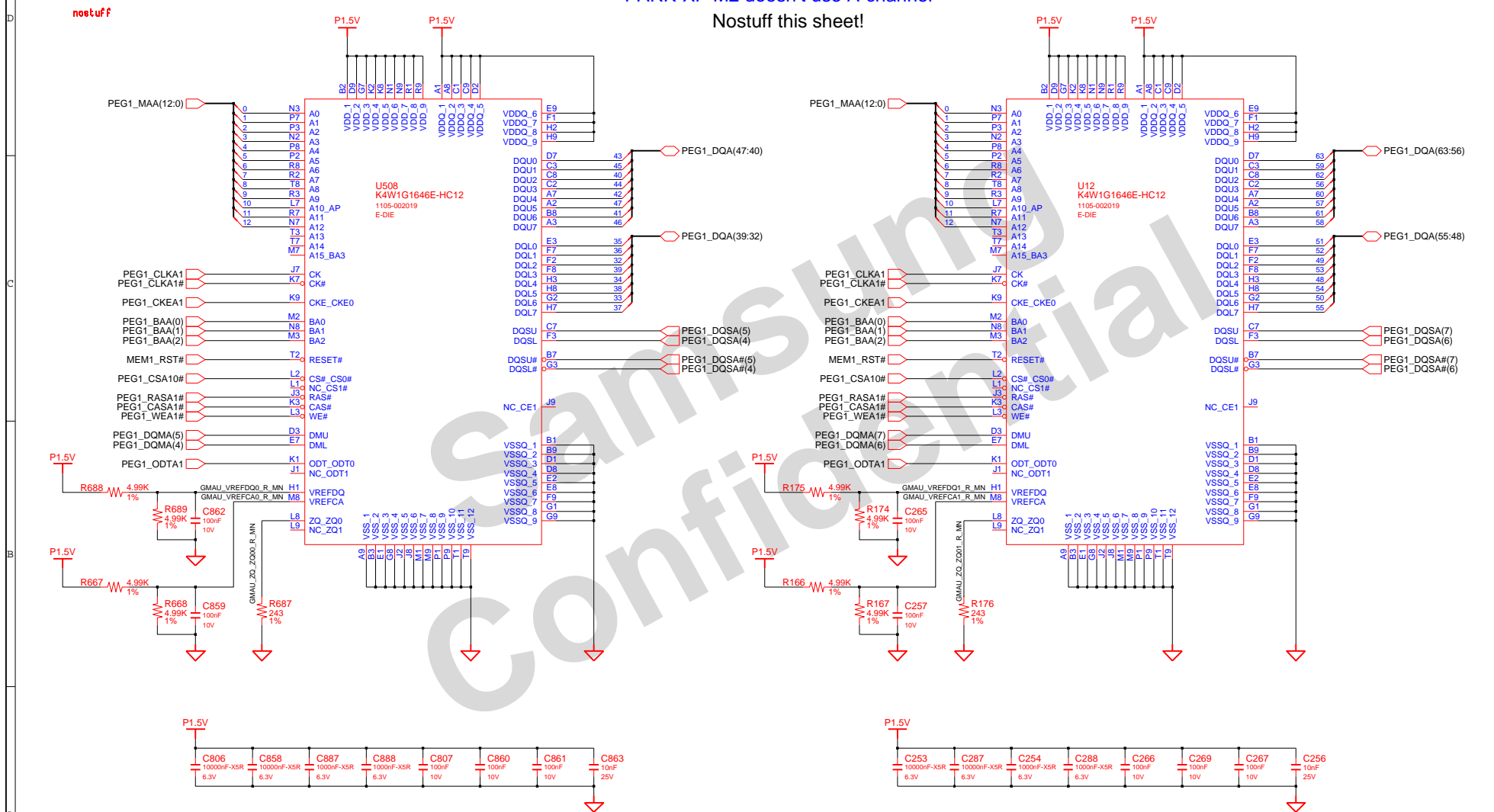
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A-channel Upper Data

PARK-XP M2 doesn't use A-channel

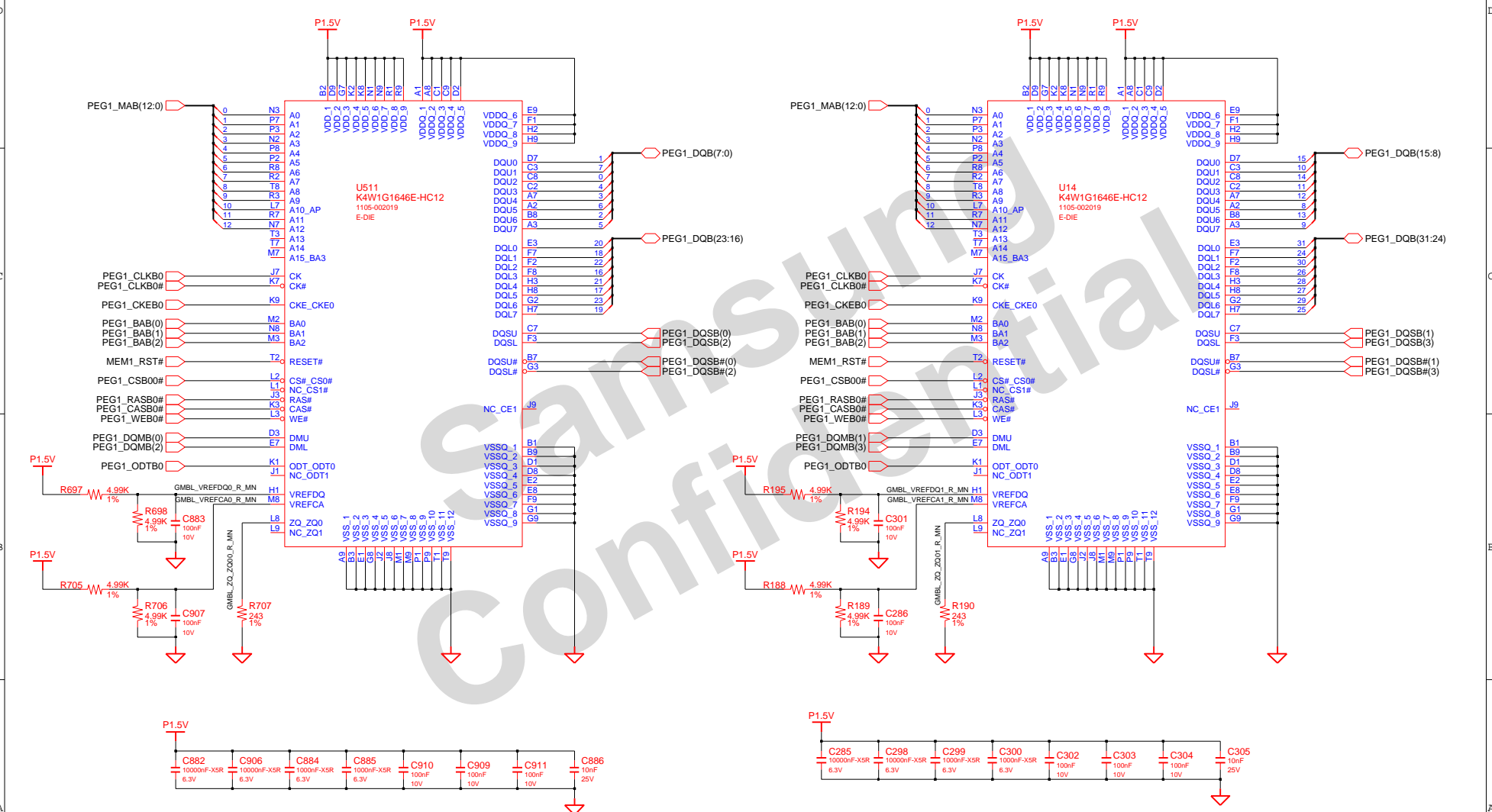
Nostuff this sheet!



PEG1_CLKA1 R178 56 1%
PEG1_CLKA1# R177 56 1%

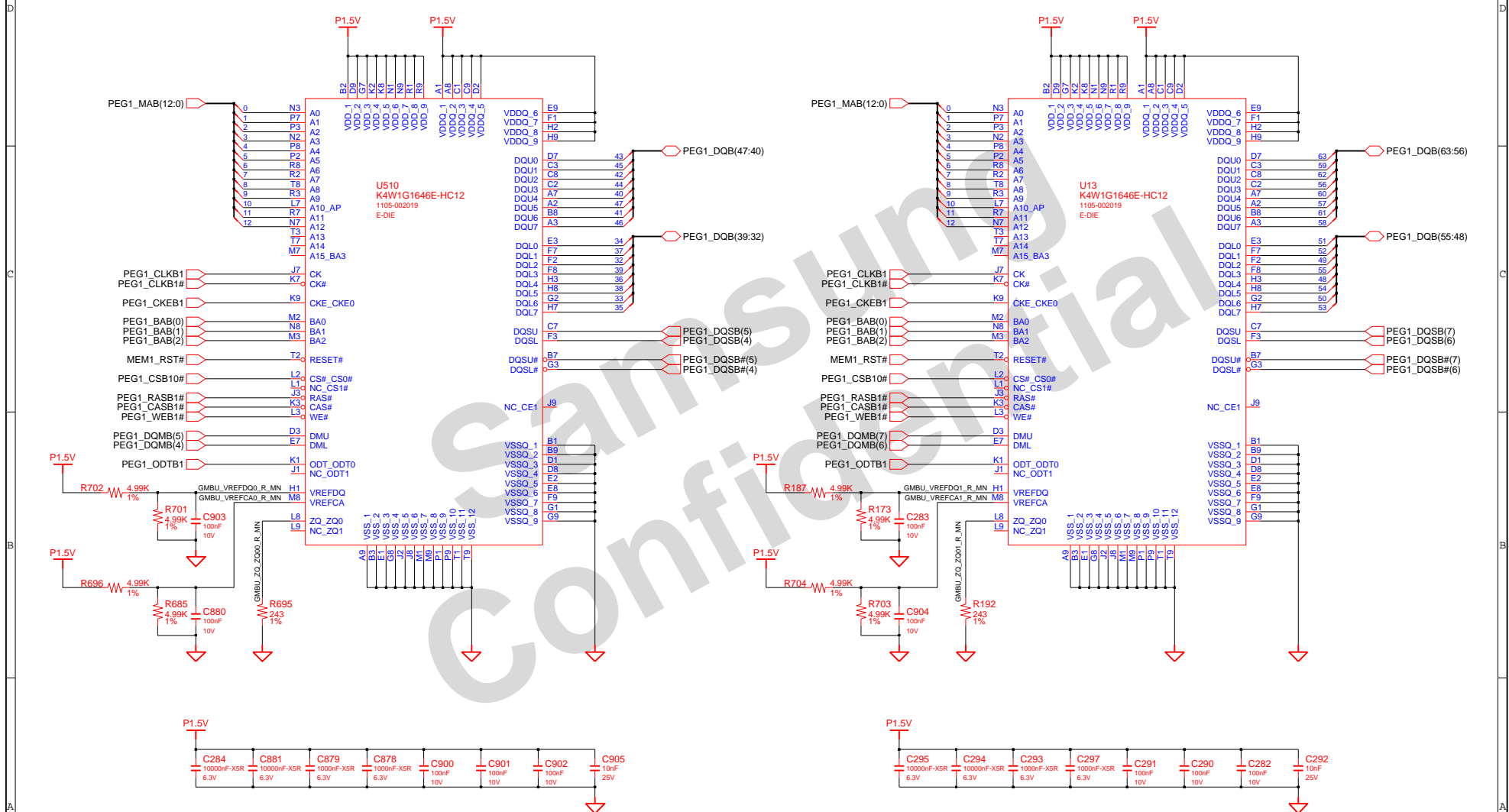
DESIGN	H.J.R	DATE	9/3/2009	TITLE	Bremen-D GRAPHICS MEMORY gDDR3	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	24 OF 61	

B-channel Lower Data



DESIGN	H.J.R.	DATE	9/3/2009	TITLE	Bremen-D GRAPHICS MEMORY gDDR3	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	25 OF 61	

B-channel Upper Data



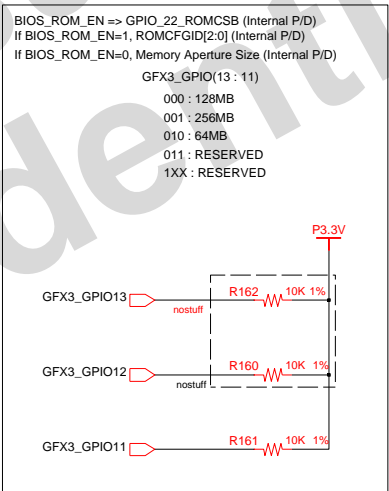
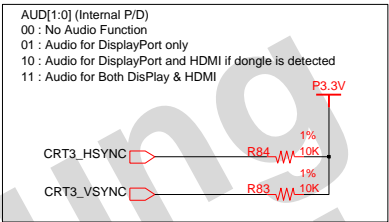
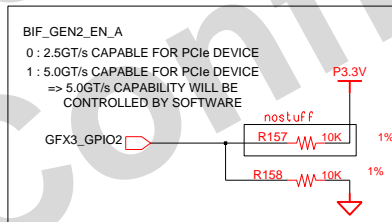
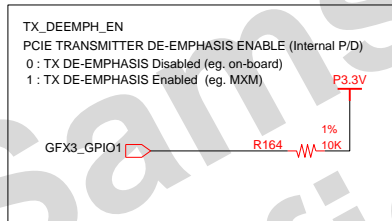
DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D GRAPHICS MEMORY gDDR3	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	26 OF 61	

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TX_PWRS_ENB
PCIE FULL TX OUTPUT SWING (Internal P/D)
0 : 50% TX OUTPUT SWING
=> LOW LOSS INTERCONNECT
1 : FULL TX OUTPUT SWING

P3.3V

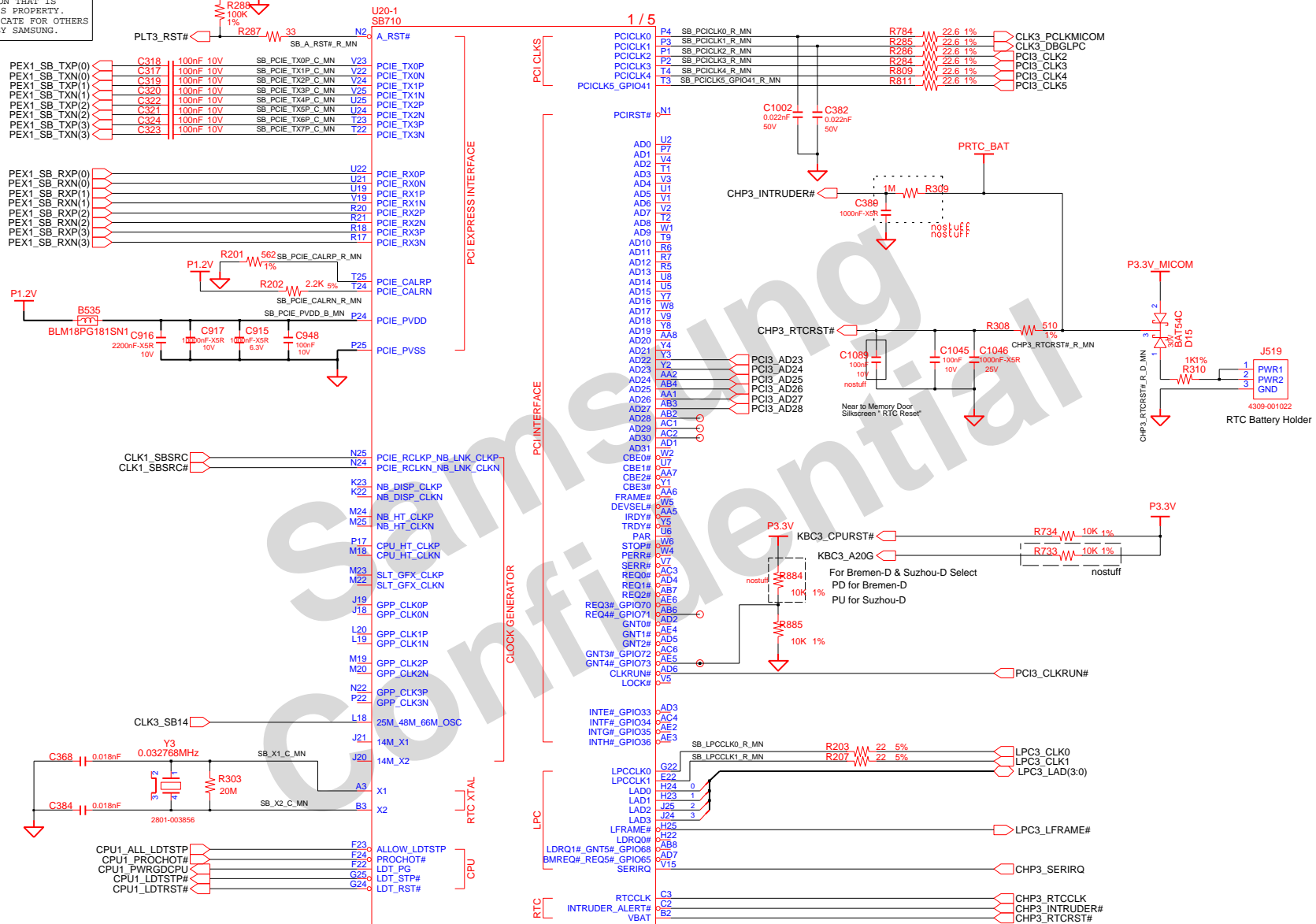
GFX3_GPIO0 R165 1% 10K



DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D GFX MADISON-LP	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE	LAST EDIT			October 10, 2009 16:50:44 PM	PAGE	27
					OF	61

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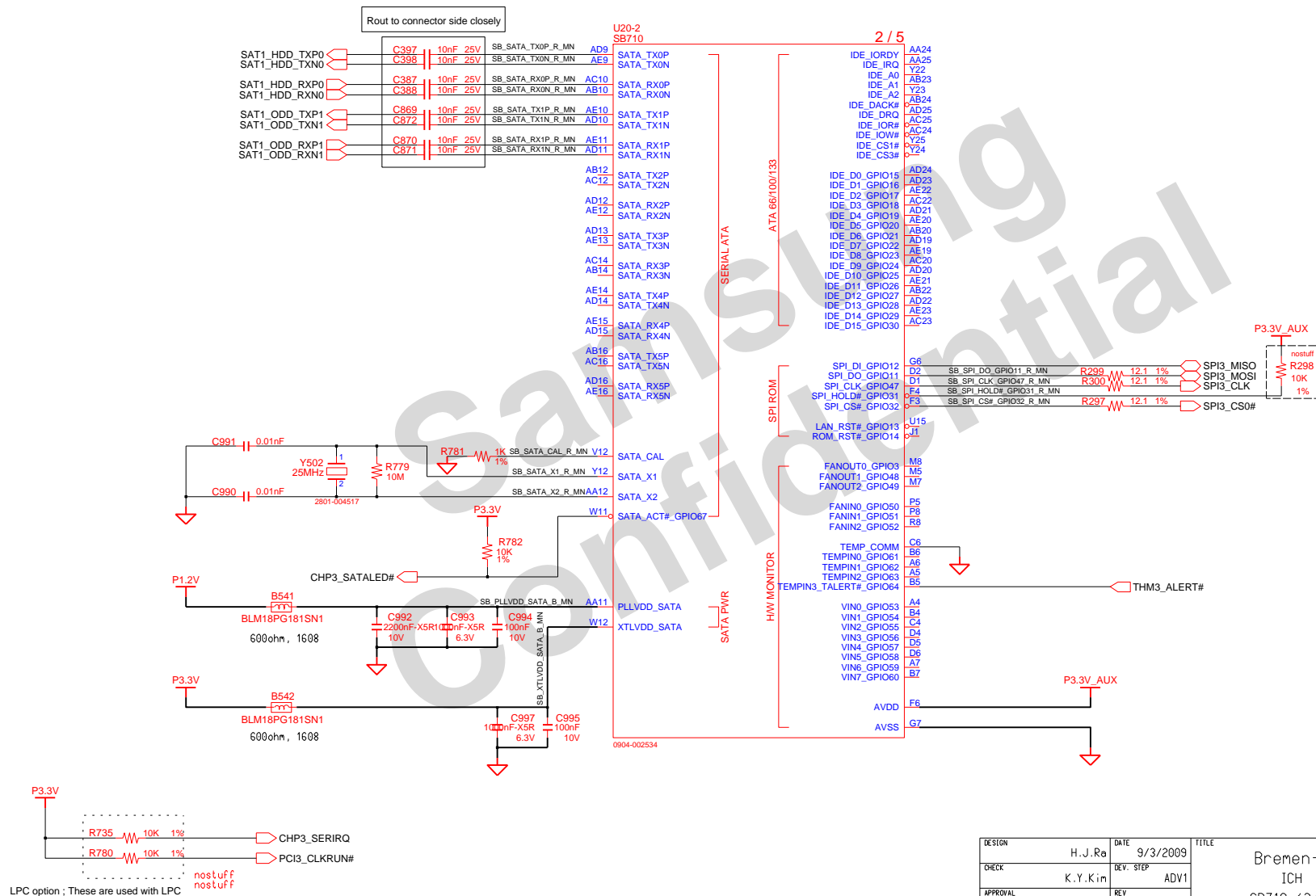
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DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D ICH SB710 (1/5)	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	28 OF 61	

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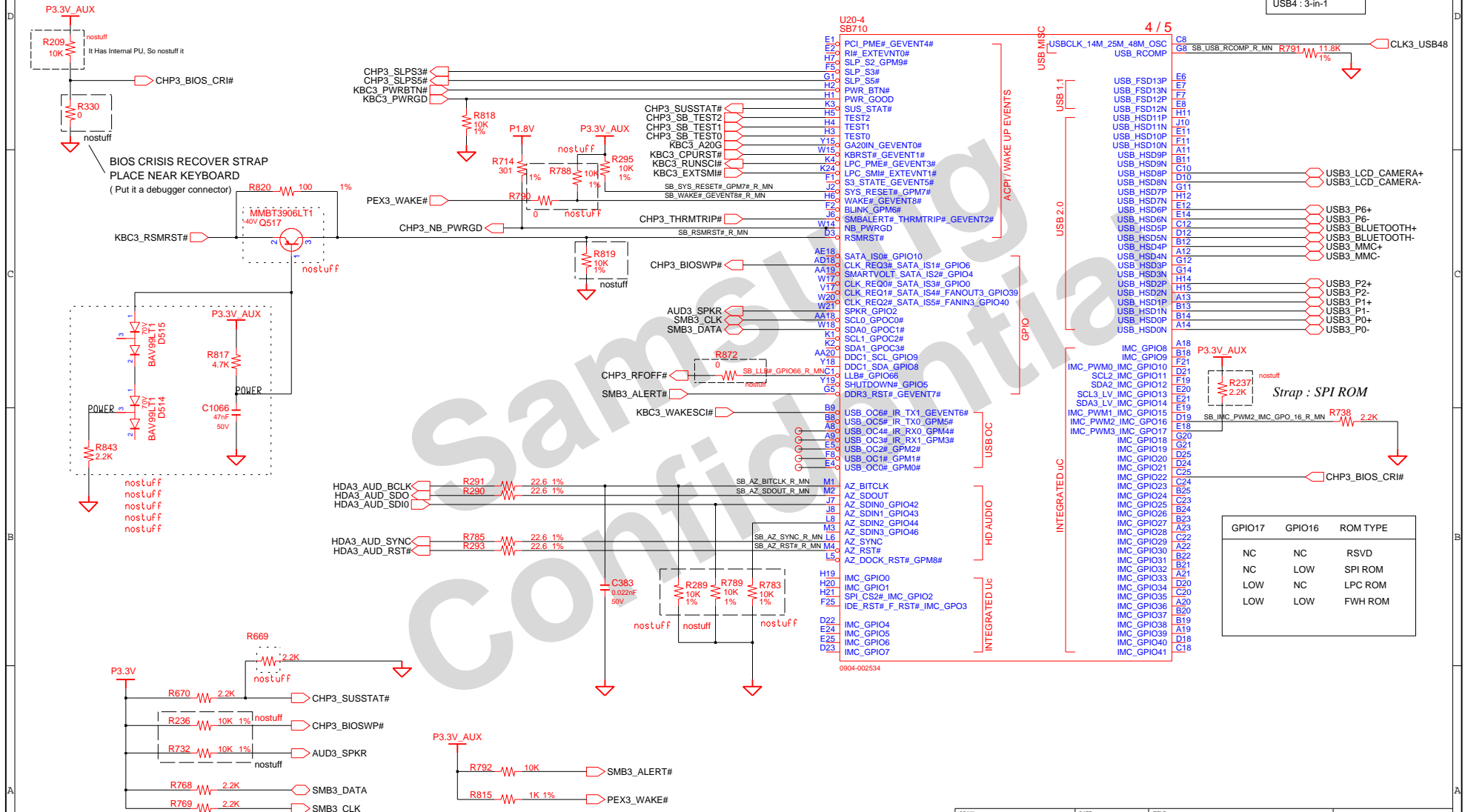


DESIGN	H.J.Ra	DATE	9/3/2009	TITLE	Bremen-D ICH SB710 (2/5)	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	29 OF 61	

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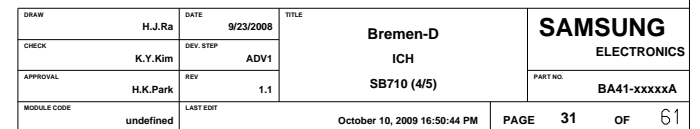
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USB1: 6: Right Port
USB0: Left Port
USB5: Bluetooth
USB8: Camera
USB4: 3-in-1

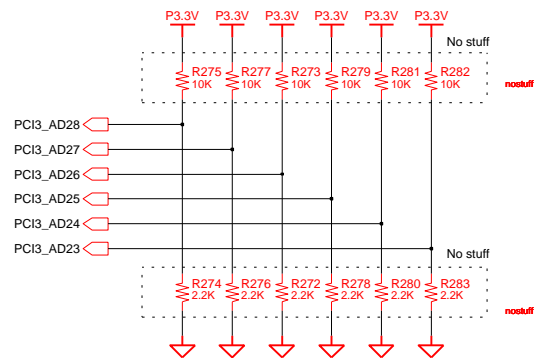


DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1	ICH		
APPROVAL	H.K.Park	REV	1.1	SB710 (3/5)	PART NO.	
MODULE CODE		LAST EDIT			BA41-xxxxxxA	
October 10, 2009 16:50:44 PM						PAGE 30 OF 61

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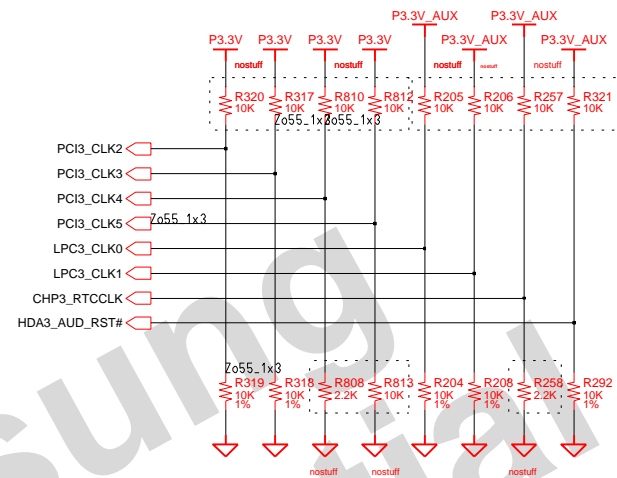


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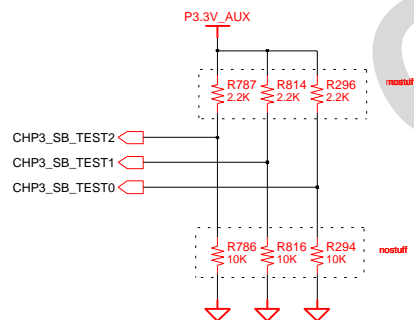


DEBUG STRAPS

	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED



	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	LPC3_CLK0	LPC3_CLK1	RTC_CLK	AUD_RST#
STRAP HIGH	BOOTFAIL TIMER ENABLED	USER DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT
STRAP LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS	RESERVED	RESERVED	EC DISABLED	CLKGEN DISABLED	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT

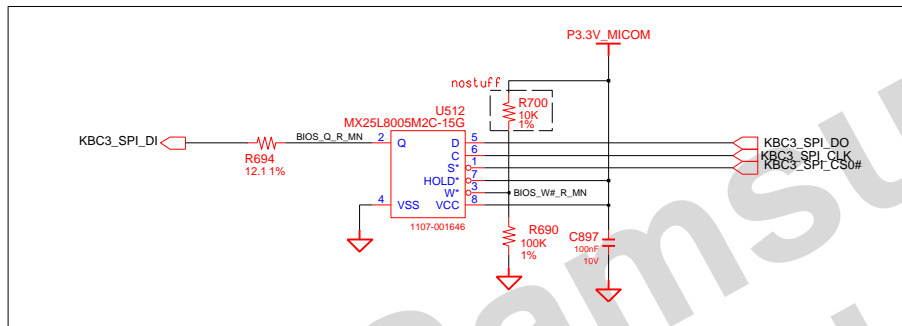


Remove SB_TEST pins for mass production. (For ASIC debug only - AMD)

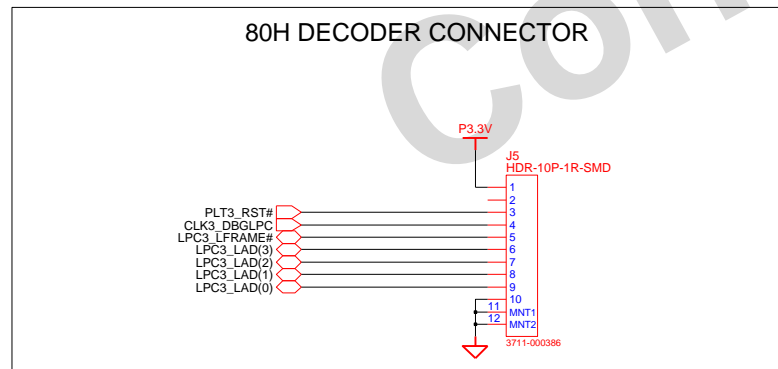
DRAW	H.J.Ra	DATE	9/23/2008	Bremen-D ICH SB710 STRAPS (5/5)		SAMSUNG ELECTRONICS			
CHECK	K.Y.Kim	DEV. STEP	ADV1						
APPROVAL	H.K.Park	REV	1.1						
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM		PAGE	32	OF	61

SPI_BIOS_ROM

8MBit

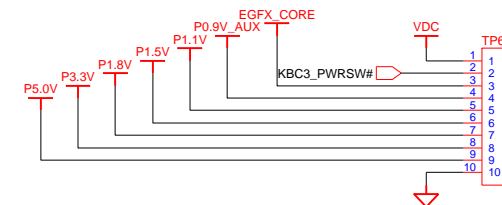


80H DECODER CONNECTOR



02 VERIFY REAL MODE
03 DISABLE NMI
04 GET CPU TYPE
06 INIT SYSTEM H/W
08 INIT CHIPSET REG.
09 SET IN POST FLAG
0A INIT CPU REG
0B CPU CACHE ON
0C INIT CACHE TO POST
0E INIT I/O VALUE
0F ENABLE THE L-BUS IDE
10 INIT POWER MANAGER
11 LOAD ALTERNATE REG
13 PCI BUS MASTER RESET
WITH INITIAL POST VALUE
14 INIT KEYBOARD CONTROLLER
16 CHECK CHECKSUM
18 8254 TIMER INIT
1A 8237 DMA CONTROLLER INIT
1C RESET INTERRUPT CONTROLLER
20 TEST DRAM REFRESH
22 TEST 8742 KEYBOARD CONTROLLER
24 SET ES SEGMENT REG. TO 4GB
26 ENABLE A20
28 AUTO SIZING DRAM
32 COMPUTE THE CPU SPEED
34 TEST CMOS RAM
38 SHADOW SYSTEM BIOS ROM
3A AUTO SIZING CACHE
3C CONFIGURE ADVANCED CHIPSET REG.
3D LOAD ALTER REG. WITH CMOS VALUE
42 INIT I/O INTERRUPT
44 CHECK ROM COPYRIGHT NOTICE
46 INIT I20 SUPPORT IF INSTALLED
48 CHECK VIDEO CONFIGURE AGAINST CMOS
49 INIT PCI BUS AND DEVICE
4A INIT ALL VIDEO BIOS ROM
4C SHADOW VIDEO BIOS ROM
50 DISPLAY CPU TYPE AND SPEED
52 TEST KEYBOARD
54 SET KEYCLICK IF ENABLED
56 ENABLE KEYBOARD
58 TEST FOR UNEXPECTED INTERRUPTS
5A DISPLAY *PRESS* SETUP*
5C TEST RAM BETWEEN 512K AND 640K
60 TEST EXTENDED MEMORY
62 TEST EXTENDED MEMORY ADDRESS LINE
64 JUMP TO USER PATCH 1
66 CONFIGURE ADVANCE CACHE REG.
6A DISPLAY EXTERNAL CACHE SIZE
6C DISPLAY SHADOW MESSAGE
6E DISPLAY NON-DISPOSABLE SEGMENT
70 DISPLAY ERROR MESSAGE
72 CHECK FOR CONFIGURATION ERROR
74 TEST REAL-TIME CLOCK
76 CHECK FOR KEYBOARD ERROR
78 SETUP HARDWARE INTERRUPT VECTOR
7E TEST COPROCESSOR IF PRESENT
80 DISABLE ON-BOARD I/O PORT
82 DETECT AND INSTALL EXT RS232C
84 DETECT AND INSTALL EXT PARALLEL
86 RE-INIT ON-BOARD I/O PORT
88 INIT BIOS DATA ROM
8A INIT EXTENDED BIOS DATA AREA
8C INIT FDD CONTROLLER
8E SHADOW OPTION ROMS
9C SETUP POWER MANAGEMENT
9E ENABLE H/W INTERRUPT
A0 SET TIME OF DAY
A4 INIT TYPEMATIC RATE
A8 ERASE F2 PROMPT
AA SCAN FOR F2 KEY STROKE
AC ENTER SETUP
AE CLEAR IN POST FLAG
B0 CHECK FOR ERRORS
B2 POST DONE-PREPARE TO BOOT O/S
B4 ONE BEEP
B6 CHECK PASSWORD (OPTION)
B7 ACPI INIT
BA DIMM INIT
BE CLEAR SCREEN
C0 TRY BOOT WITH INT19
C2 INTERRUPT HANDLER ERROR
C4 UNKNOWN INTERRUPT ERROR
C6 PENDING INTERRUPT ERROR
D6 SHUTDOWN 5
D8 SHUTDOWN ERROR
DA EXTENDED BLOCK MOVE
DC SHUTDOWN 10
DE ENABLE NMI
E0 INIT HDD CONTROLLER
E2 INIT LOCAL BUS HDD CONTROLLER
E4 JUMP TO USER PATCH 2
E6 DISABLE A20 ADDRESS LINE
E8 CLEAR HUGE ES SEGMENT REG.
EA SEARCH FOR OPTION ROMS

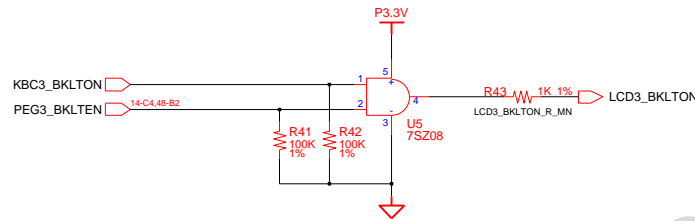
Pins for ICT FREE
should be rearranged. ICT FREE



DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1		SPI_BIOS_ROM	ELECTRONICS
APPROVAL	H.K.Park	REV	1.1		SPI_BIOS_ROM	PART NO.
MODULE CODE		LAST EDIT				BA41-xxxxxA
October 10, 2009 16:50:44 PM						PAGE 33 OF 61

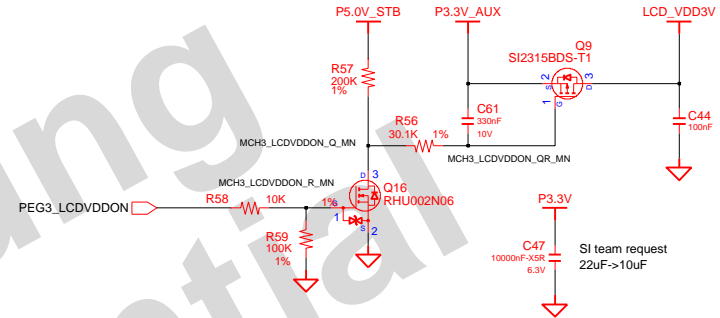
LVDS

Backlight On

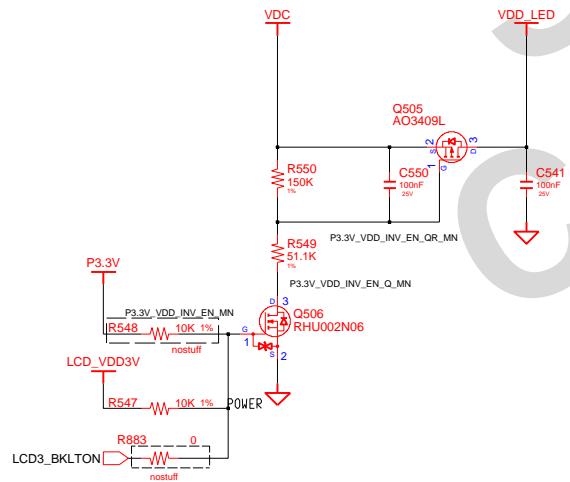


LCD Power

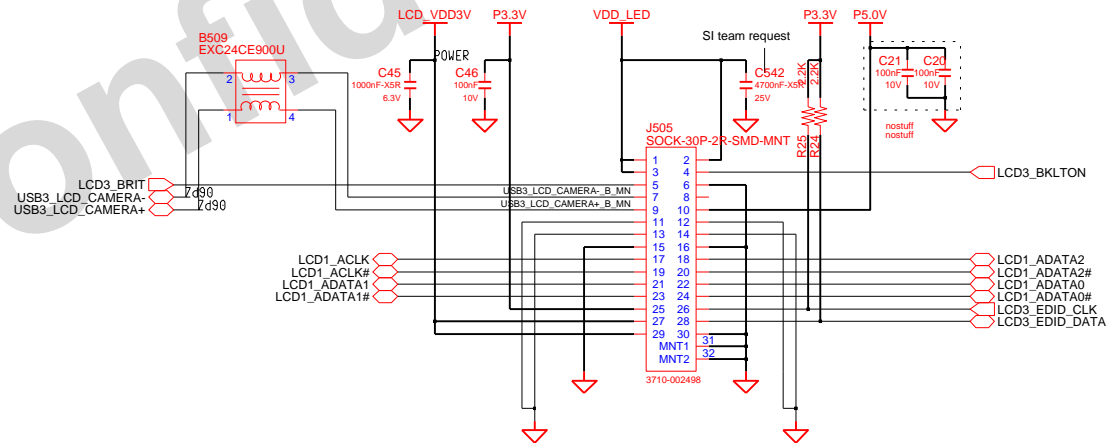
EBL Purpose



LED Power



Camera + LCD Connector



DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1	GRAPHICS_IF	
APPROVAL	H.K.Park	REV	1.1	LVDS	
MODULE CODE		LAST EDIT			
				October 10, 2009 16:50:44 PM	PAGE 34 OF 61

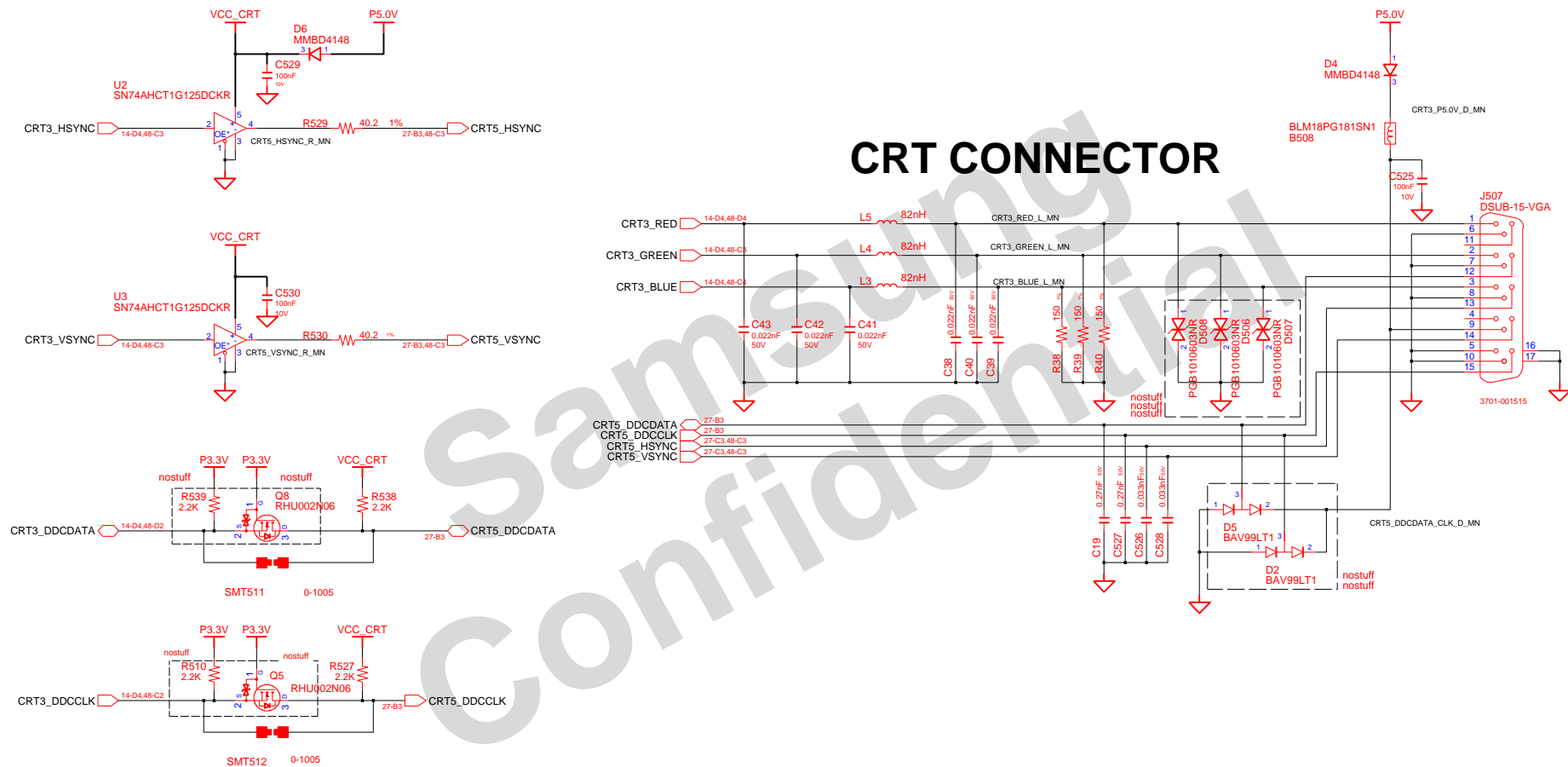
SAMSUNG
ELECTRONICS
PART NO. BA41-xxxxxA

CRT

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CRT

CRT CONNECTOR

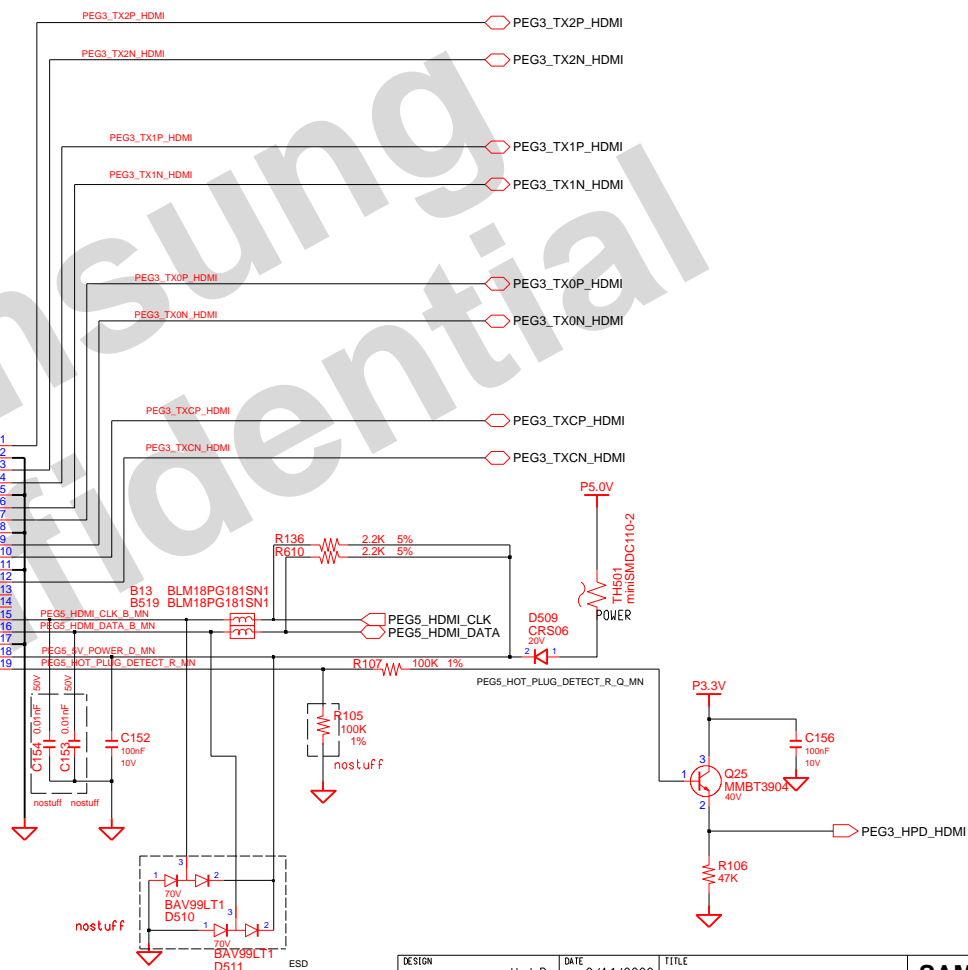
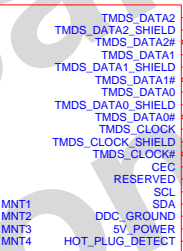
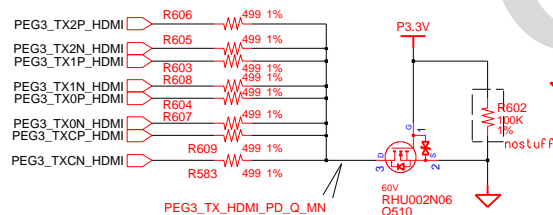
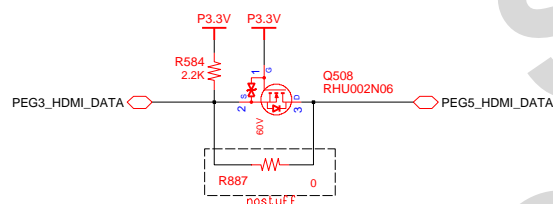


Check "CRT3_DDCCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1	GRAPHICS_IF	ELECTRONICS	
APPROVAL	H.K.Park	REV	1.1	CRT	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE	35 OF 61

HDMI

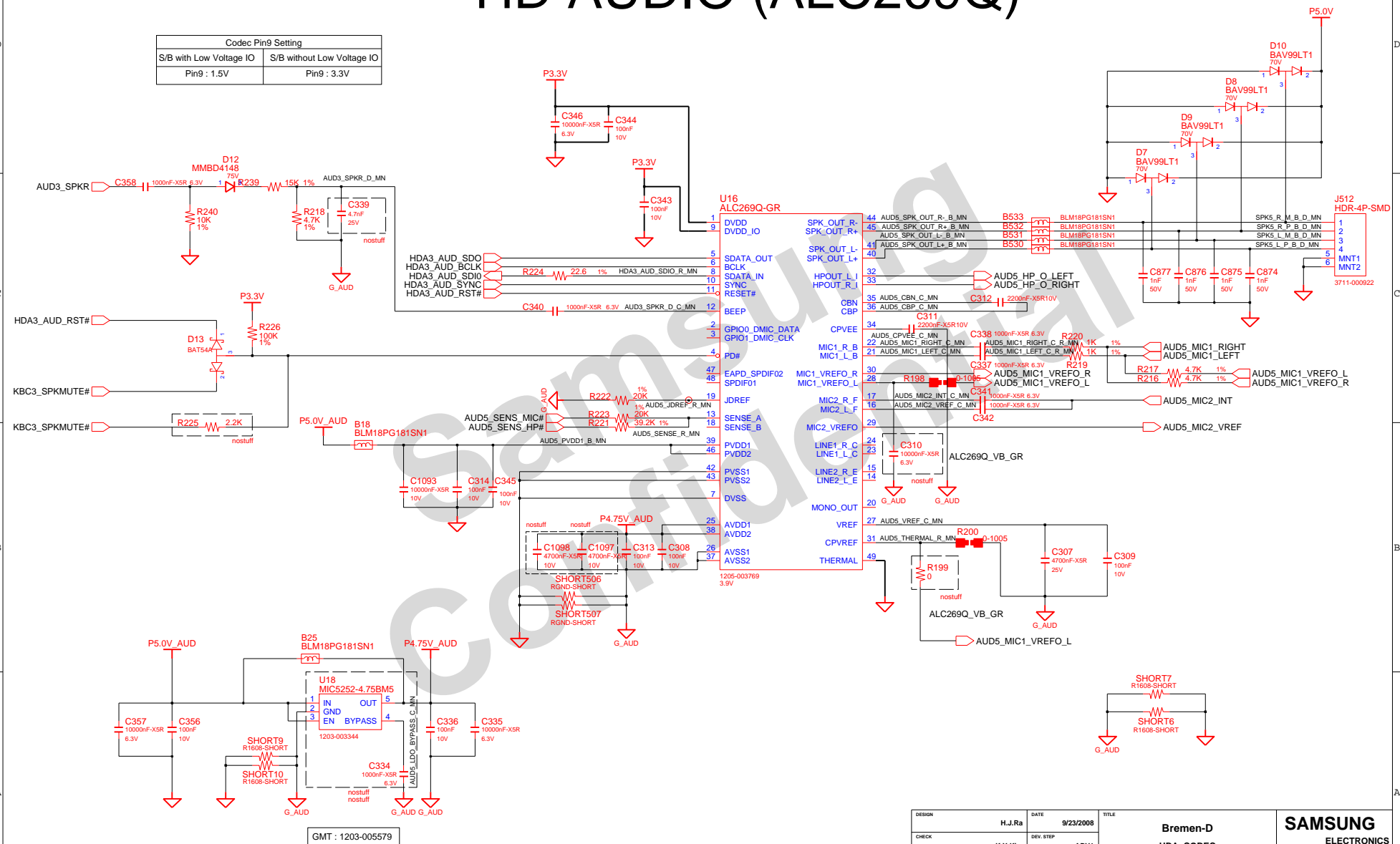
The schematic diagram illustrates the HDMI signal path. It features a differential signal line connecting PEG3_HDMI_CLK to PEG5_HDMI_CLK. A 2.2K resistor (R135) is connected to the signal line. A 6V regulator (Q30, RHU002N06) is connected to the signal line. A poststuffer circuit (R886) is connected to the signal line.



DESIGN	H.J.Rø	DATE	8/14/2009	TITLE Bremen-D HDMI HDMI	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1		
APPROVAL	H.K.Park	REV	1.1		
PART NO.		BA41-xxxxxA			
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE 36 OF 61

HD AUDIO (ALC269Q)

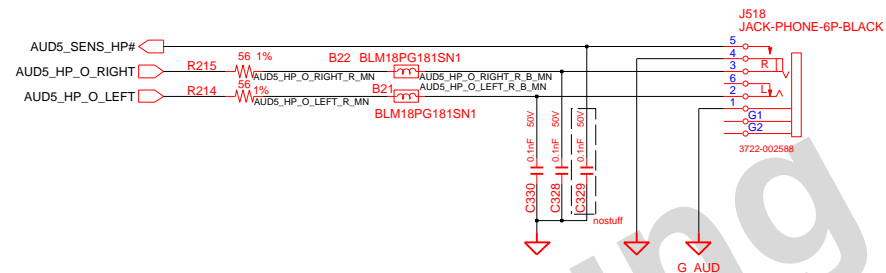
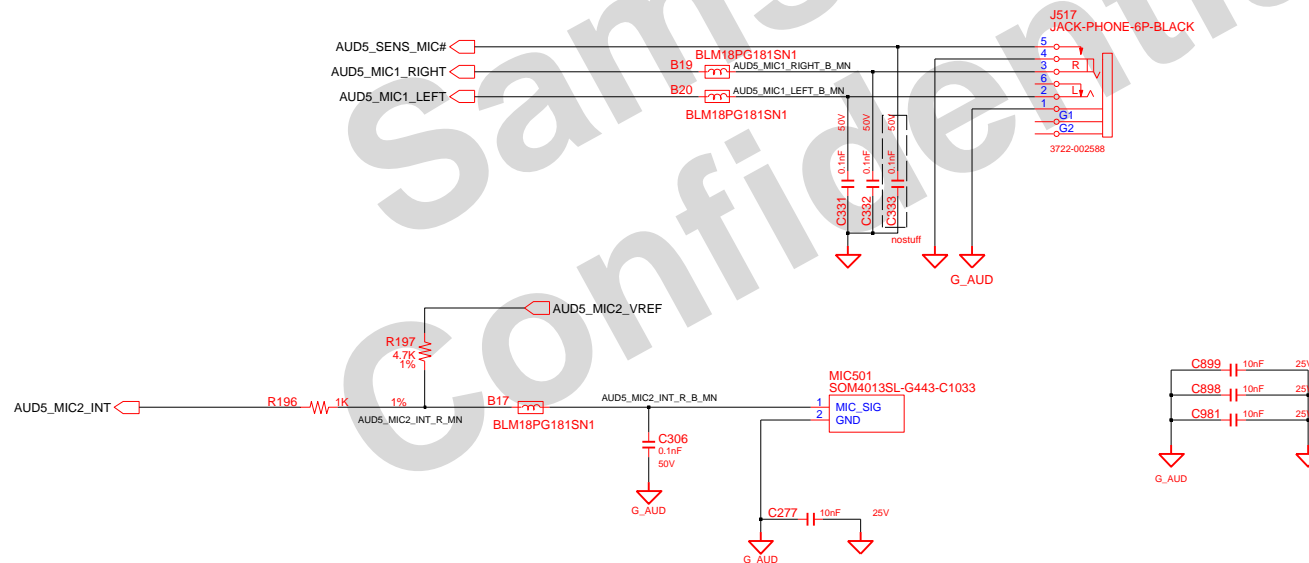
Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



DESIGN	H.J.Ra	DATE	9/23/2008	Bremen-D HDA_CODEC AUDIO CODEC ALC269Q_GR	SAMSUNG ELECTRONICS		
CHECK	K.Y.Kim	DEV. STEP	ADV1		PART NO. BA41-xxxxxxA		
APPROVAL	H.K.Park	REV	1.1				
MODULE CODE	LAST EDIT					October 10, 2009 16:50:44 PM	PAGE 37

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HEADPHONE(BLACK)**MIC JACK(BLACK)**

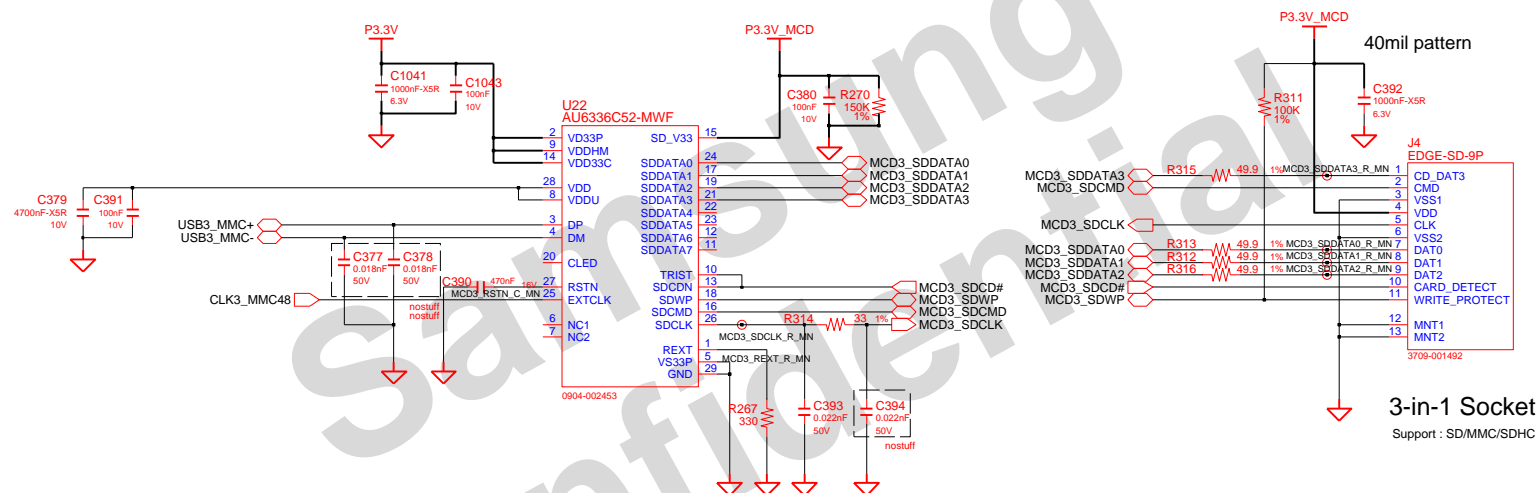
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D HDA_CODEC AUDIO INPUT/OUTPUT	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE 38 OF 61	

DESIGN	H.J.Ra	DATE	9/23/2008	Bremen-D LAN LAN_MARVELL_8040	SAMSUNG ELECTRONICS			
CHECK	K.Y.Kim	DEV. STEP	ADV1		PART NO.	BA41-xxxxxxA		
APPROVAL	H.K.Park	REV	1.1					
MODULE CODE	LAST EDIT			October 10, 2009 16:50:44 PM	PAGE	39	OF	61

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3 IN 1 CARD (AU6336)



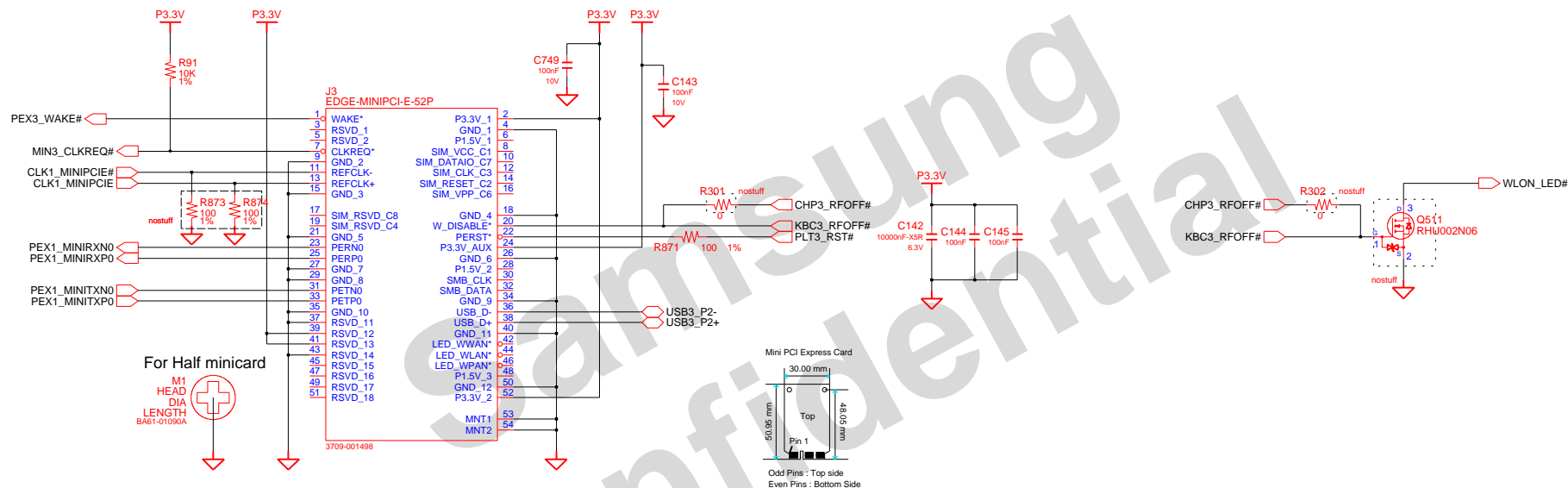
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D MULTICARD 3 IN 1 CARD	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE 40 OF 61	

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Wireless LAN

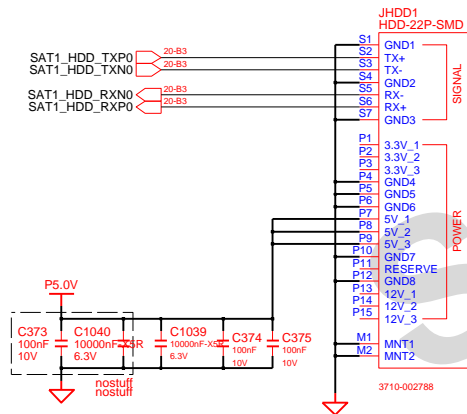
WLAN, 4mm



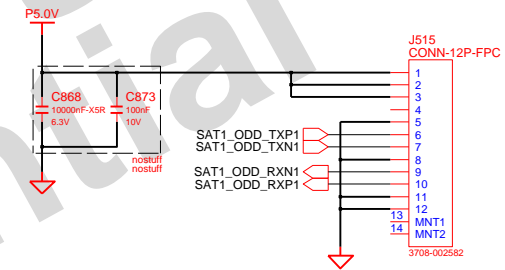
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D MINI_PCIE_CONN WLAN	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE 41 OF 61	

SATA I/F CONN

SATA HDD CONN

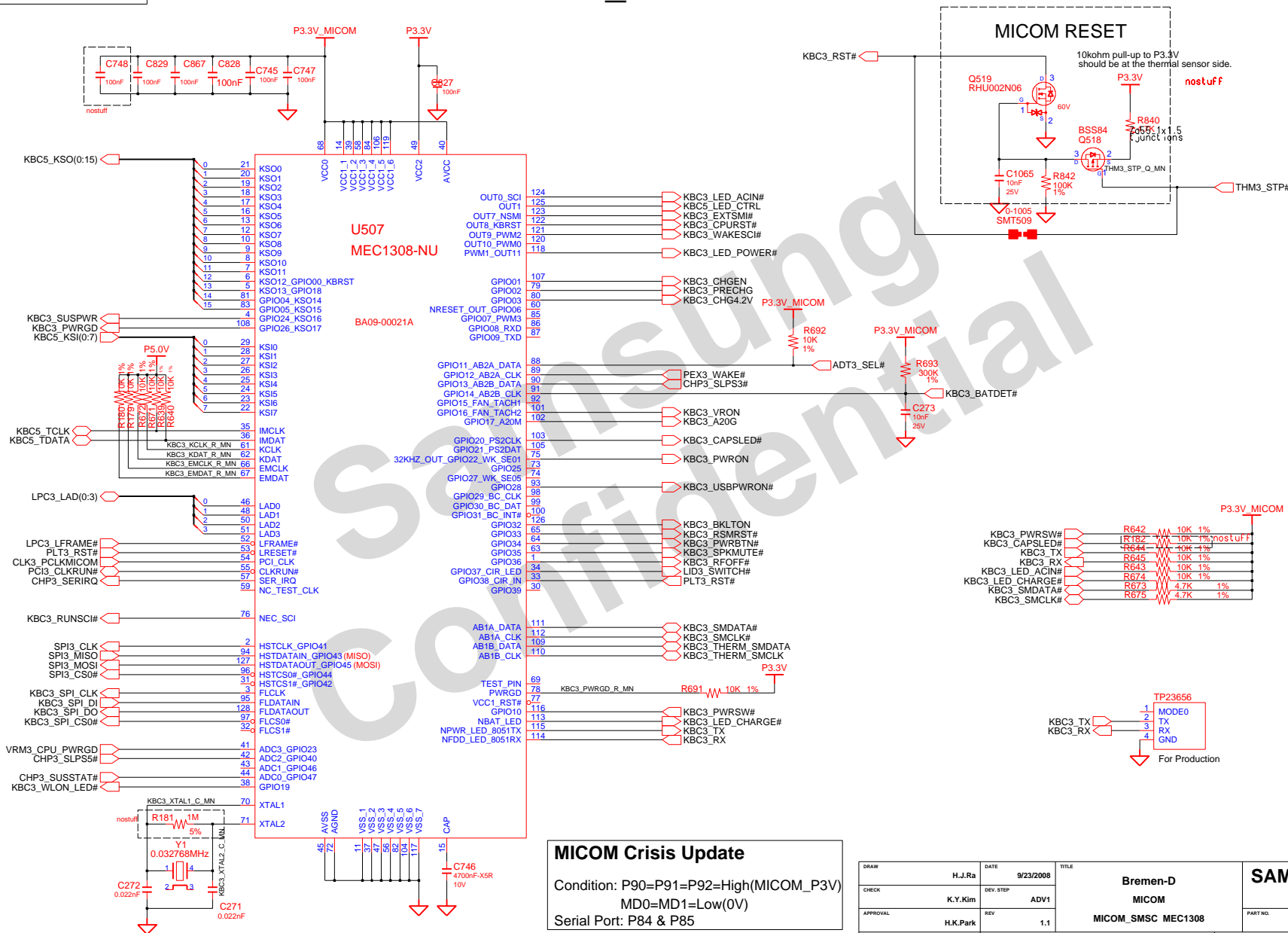


MAIN TO SUB SATA ODD CONN



DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D SATA_DEVICES	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1		HDD & ODD SUB CONNECTOR	
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	42	OF 61

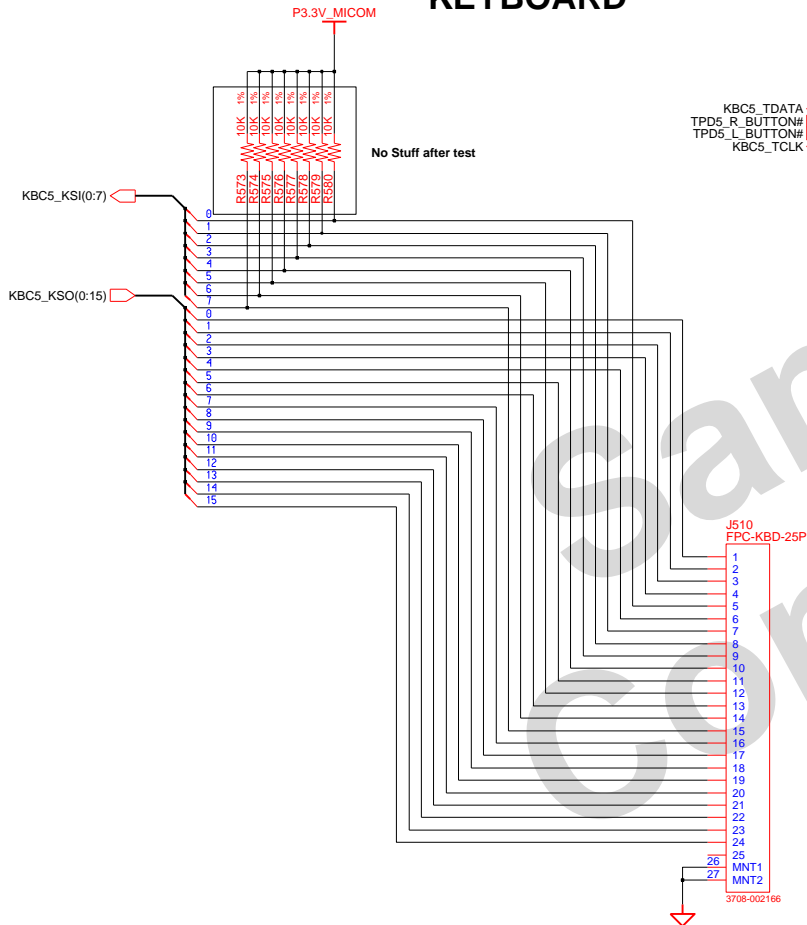
MICOM_MEC1308



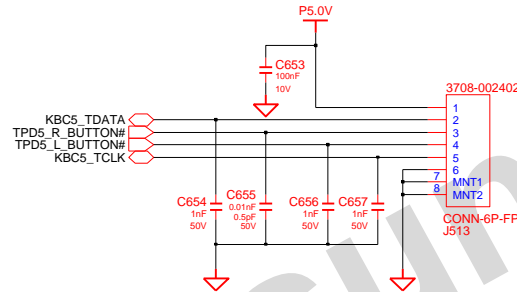
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Micom Glue Logic

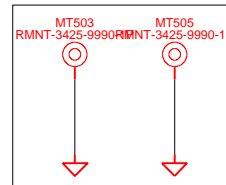
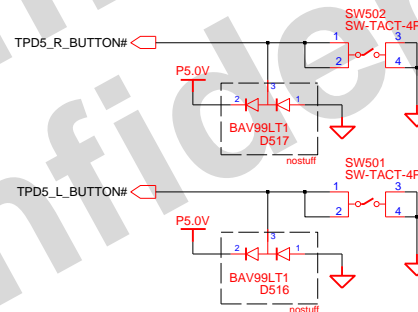
KEYBOARD



TOUCHPAD

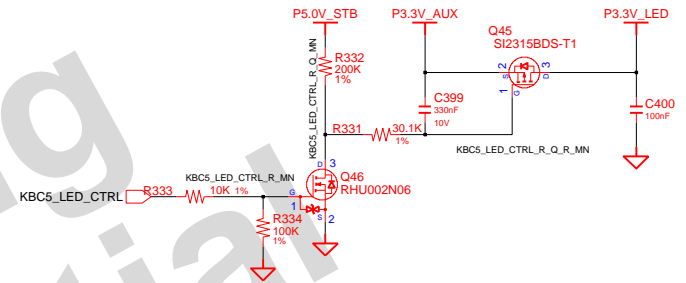


TOUCHPAD BUTTON

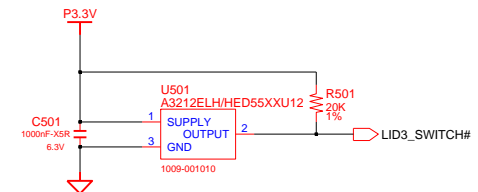


Keyboard Mount(for 15")

TOUCHPAD LED



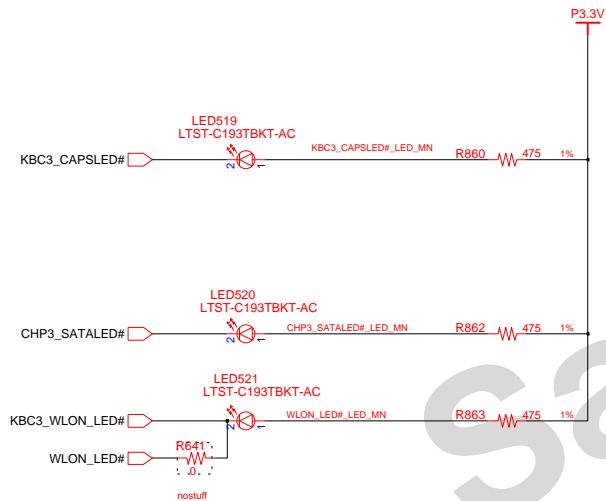
LID SWITCH



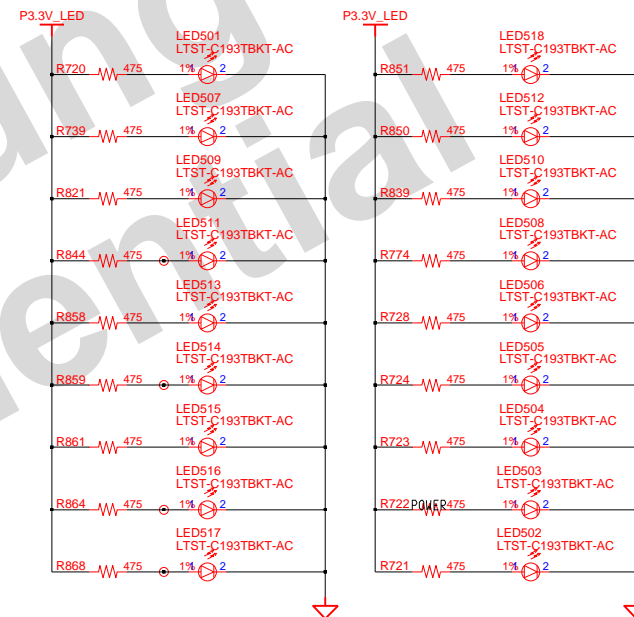
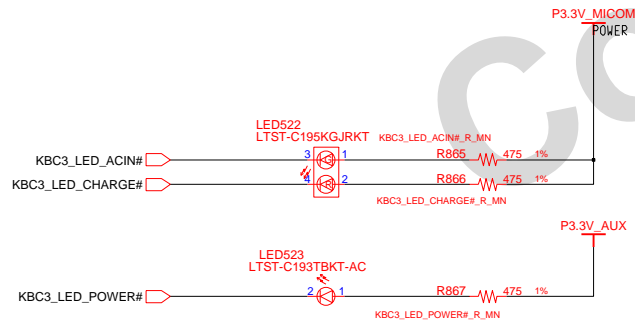
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D MICOM GLUE LOGIC KEYBOARD & TOUCHPAD	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	44	OF 61

LEDs

FUNCTION KEY LED



ADAPTERIN/CHARGING LED

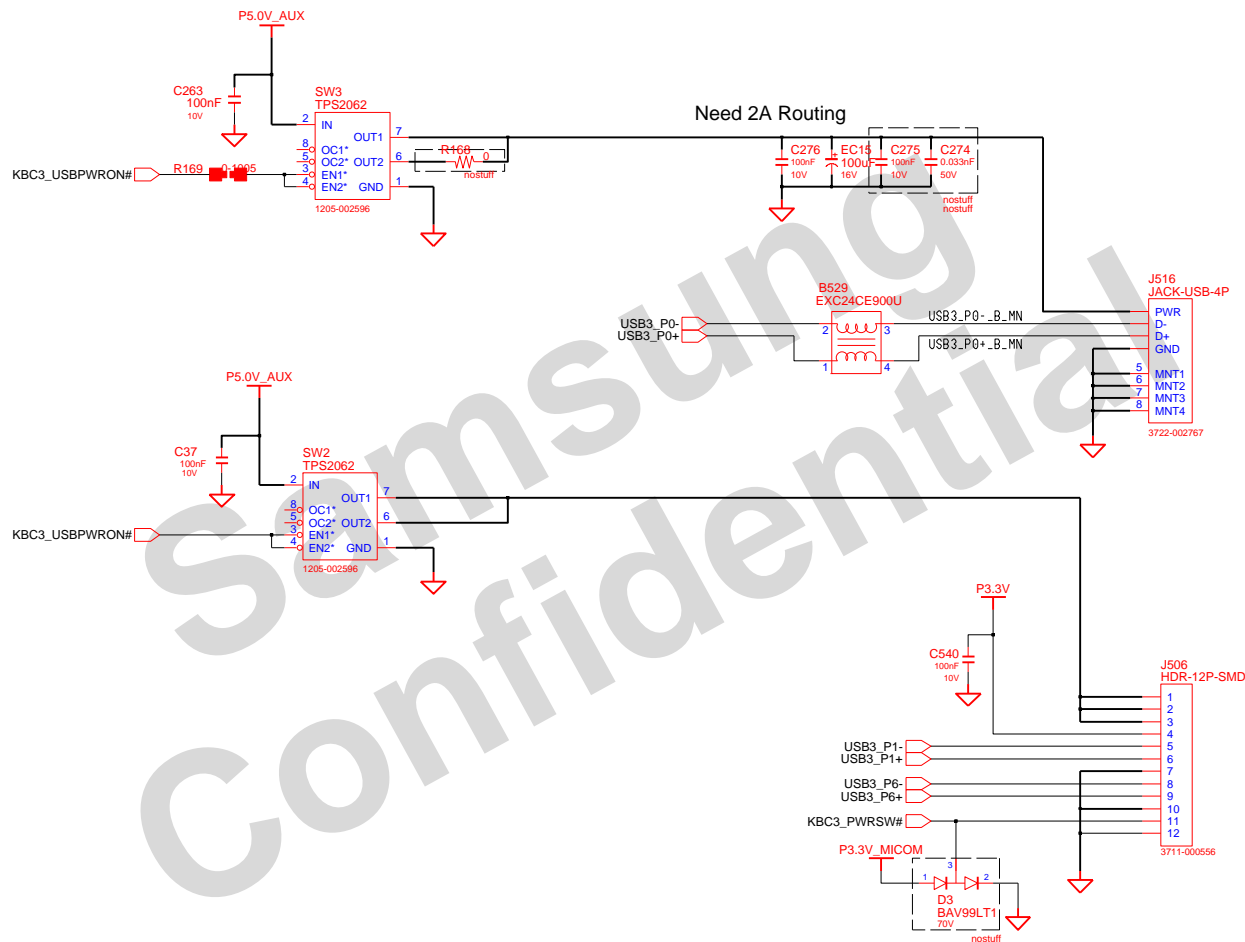


DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D LED_SWITCH	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	45	OF 61

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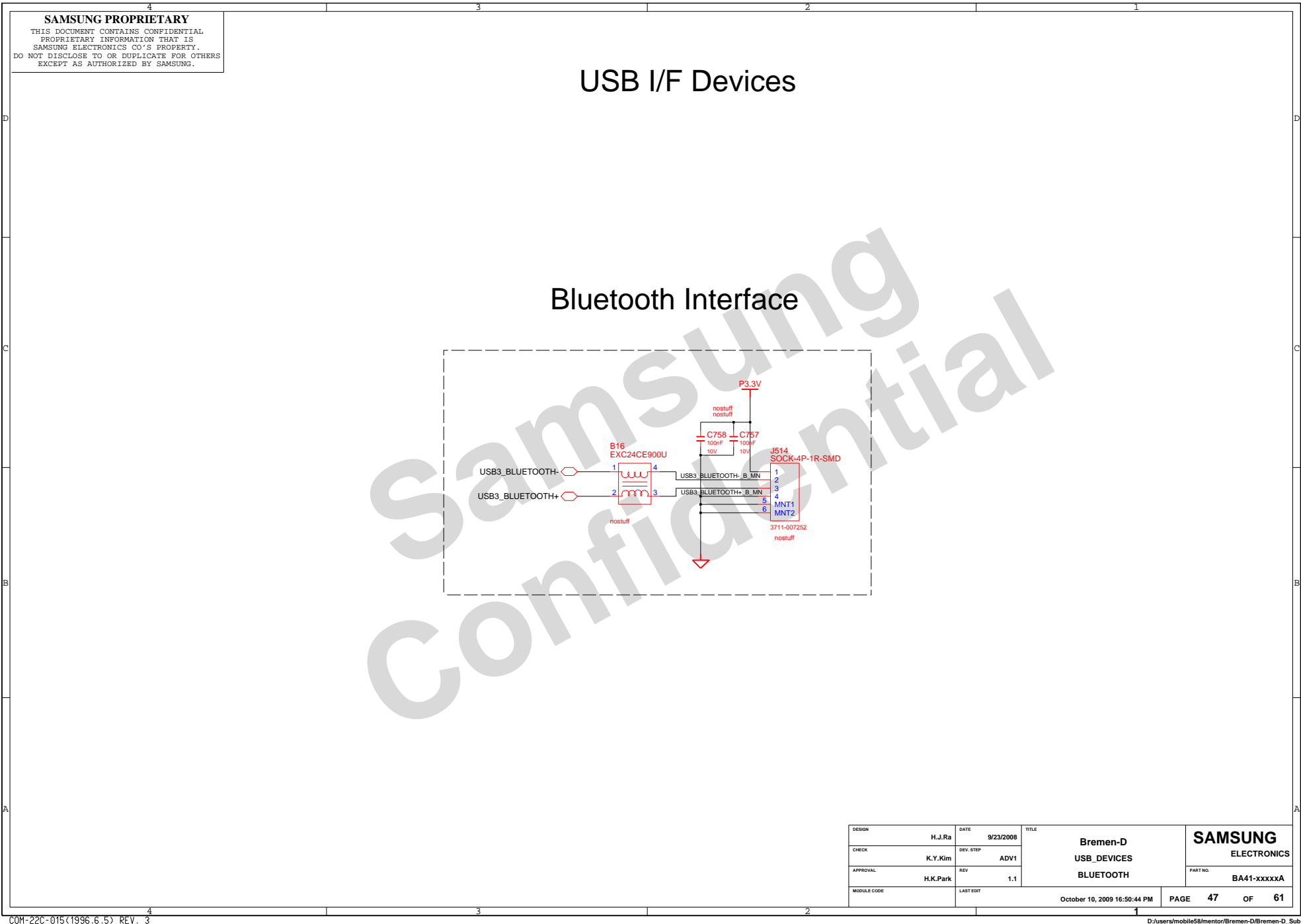
USB Single connector



DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1	USB_CONN	
APPROVAL	H.K.Park	REV	1.1	USB	
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	

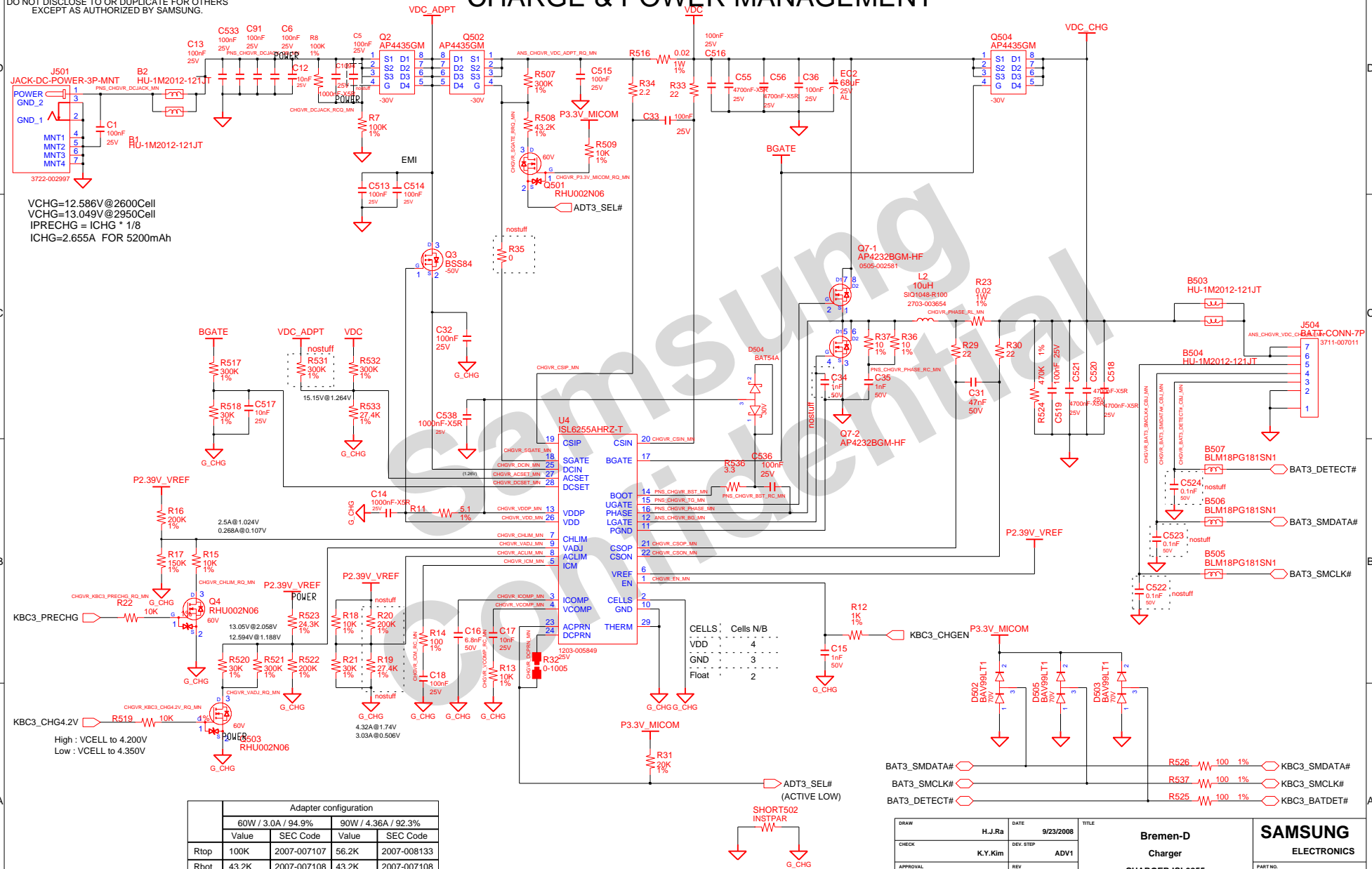
PAGE	46	OF	61
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SAMSUNG	
ELECTRONICS	
PART NO.	BA41-xxxxxA



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CHARGE & POWER MANAGEMENT

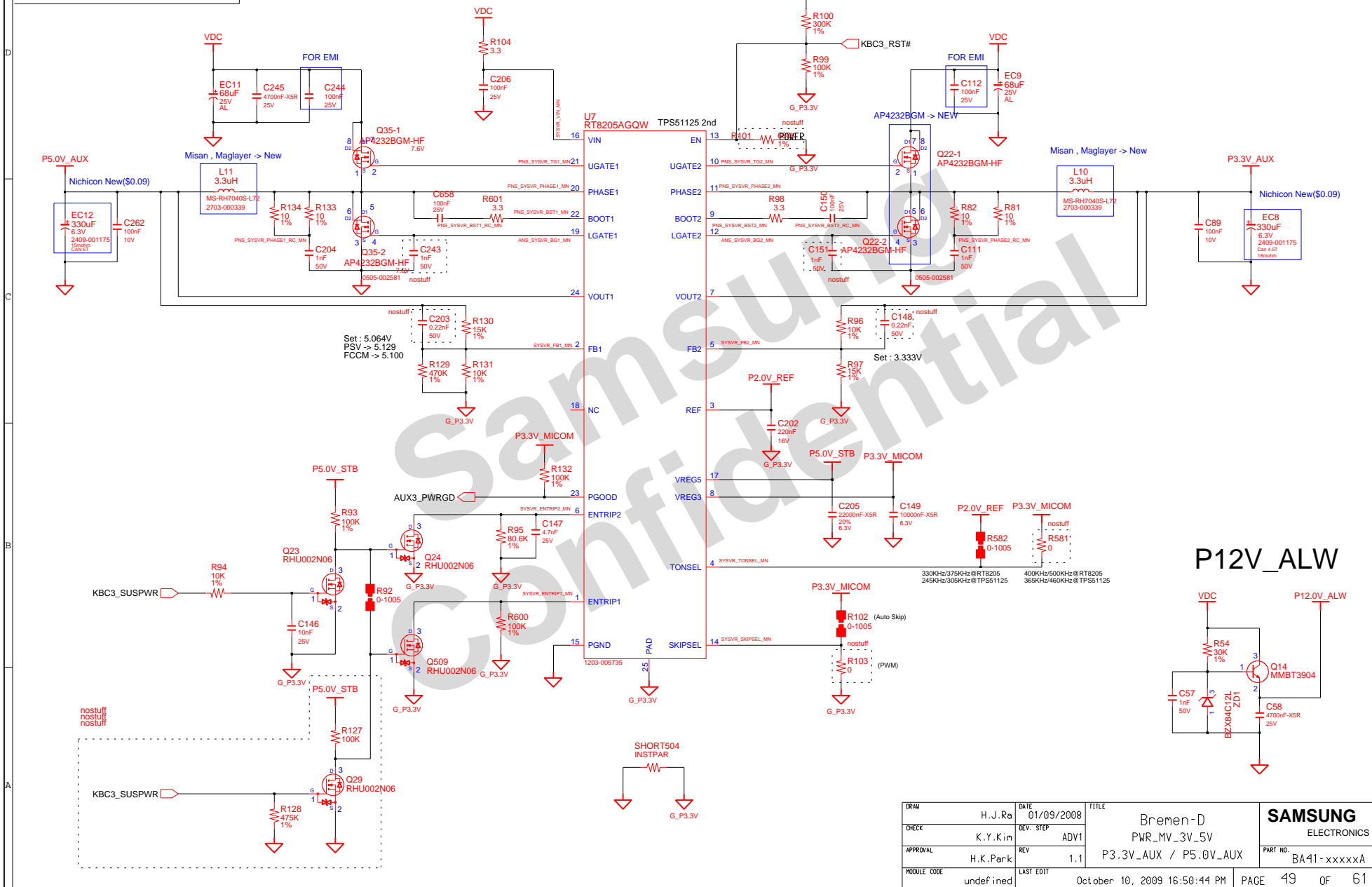


DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1		Charger
APPROVAL	H.K.Park	REV	1.1		CHARGER ISL6255
MODULE CODE	undefined	LAST EDIT			
				October 10, 2009 16:50:44 PM	PAGE 48 OF 61

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ELECTRONICS
PART NO. BA41-xxxxxA

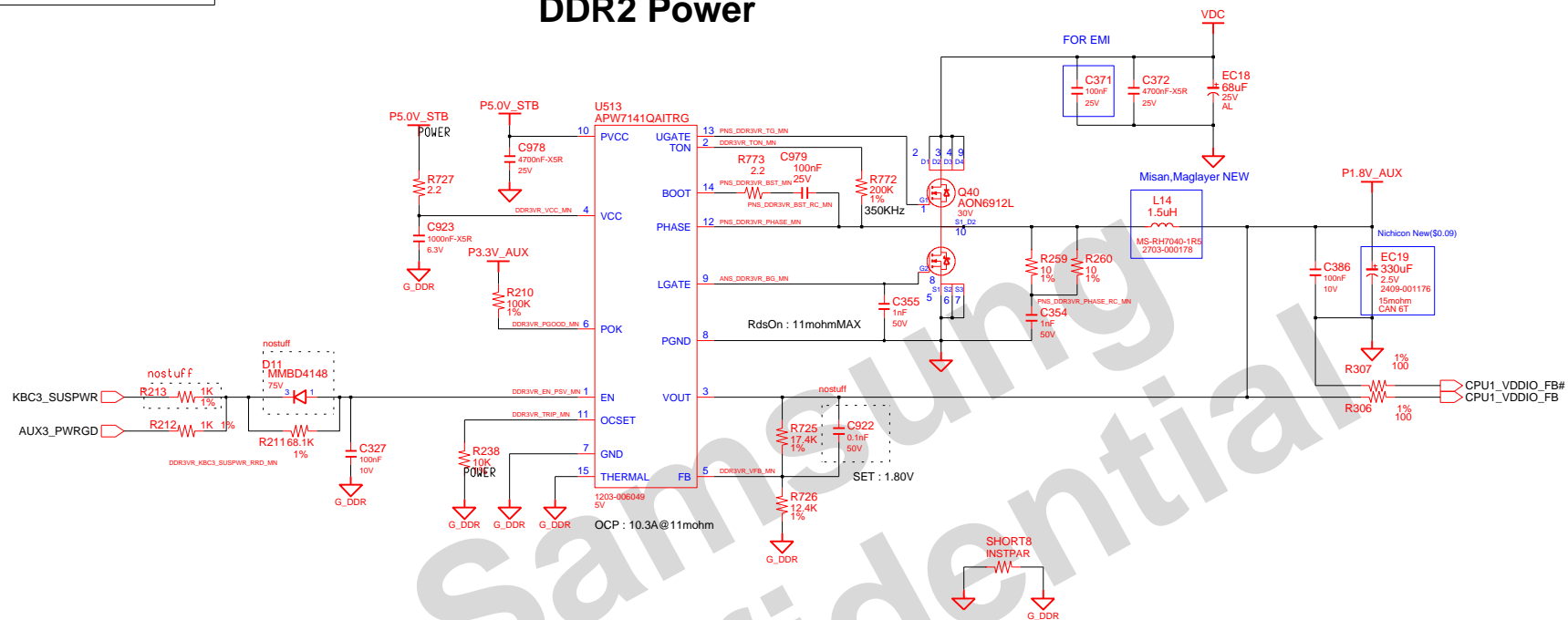
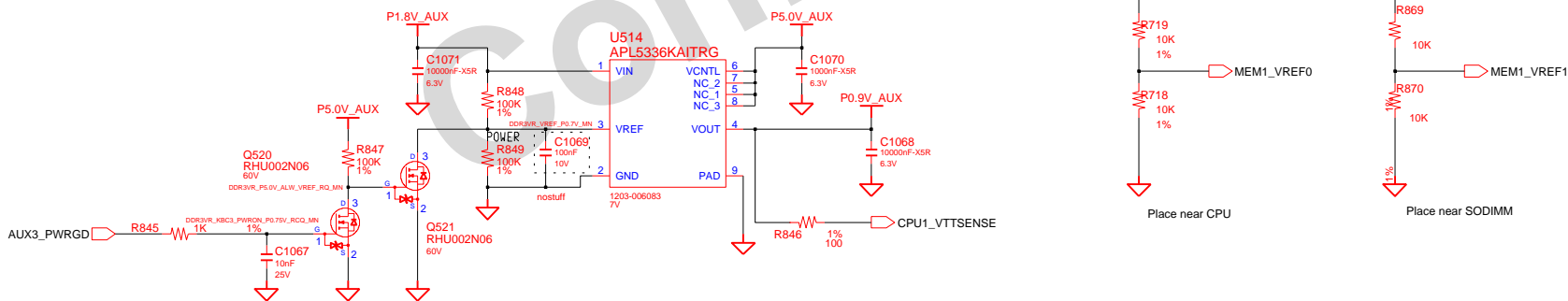
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P3.3V_AUX & P5.0V_AUX



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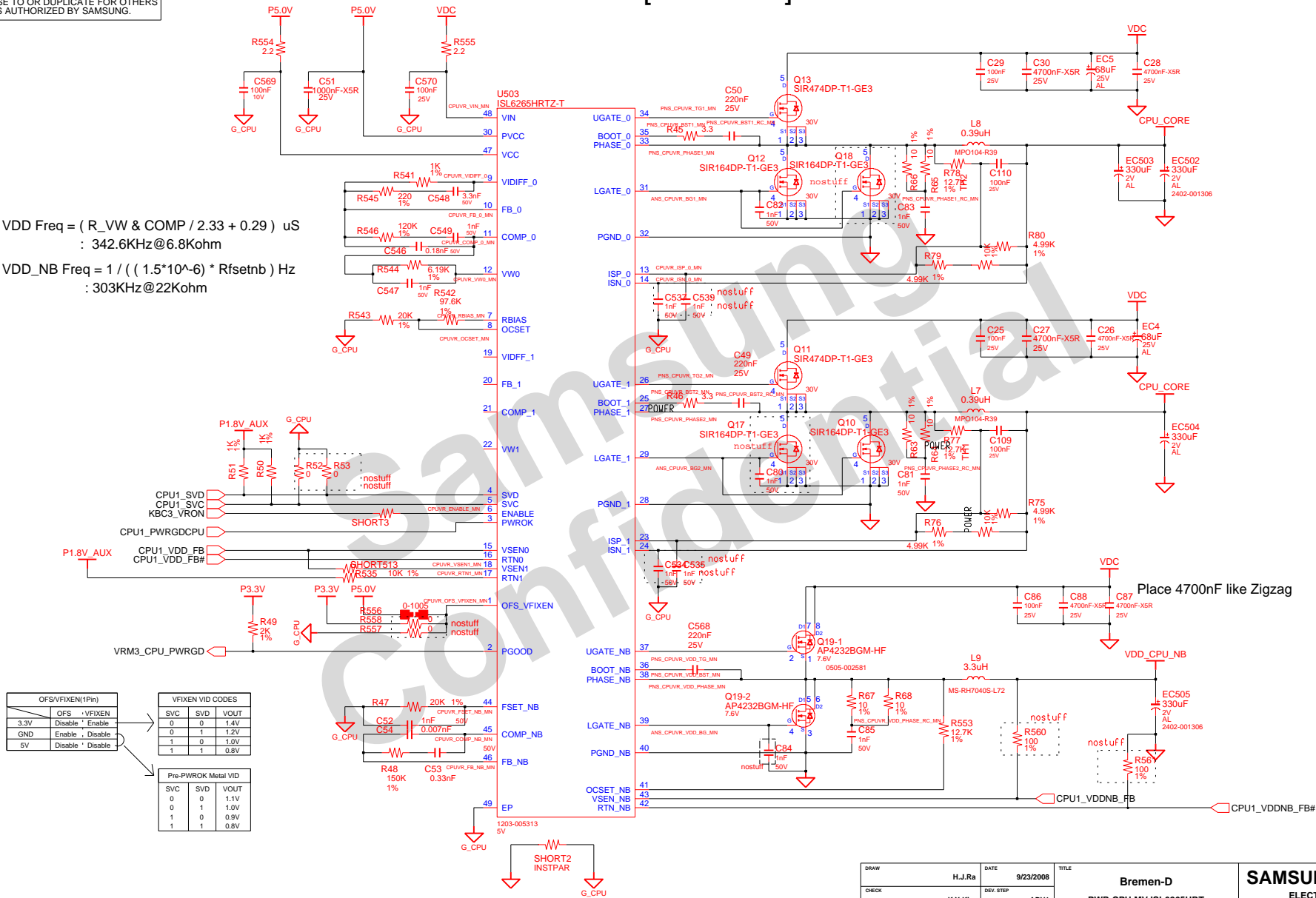
DDR2 Power**DDR2 VTT(0.9V_AUX)**

DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1	PWR_MEMORY		ELECTRONICS
APPROVAL	H.K.Park	REV	1.1	DDR2 POWER	PART NO.	BA41-xxxxxA
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	50	OF 61

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CPU VRM [INTERSIL]

$VDD \text{ Freq} = (R_VW \& COMP / 2.33 + 0.29) \text{ uS}$
: 342.6KHz@6.8Kohm
 $VDD_NB \text{ Freq} = 1 / ((1.5*10^{-6}) * Rfsetnb) \text{ Hz}$
: 303KHz@22Kohm



DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1		PWR CPU MV ISL6265HRT
APPROVAL	H.K.Park	REV	1.1		CPU VRM
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	51 OF 61

SAMSUNG	ELECTRONICS
PART NO.	BA41-xxxxxA

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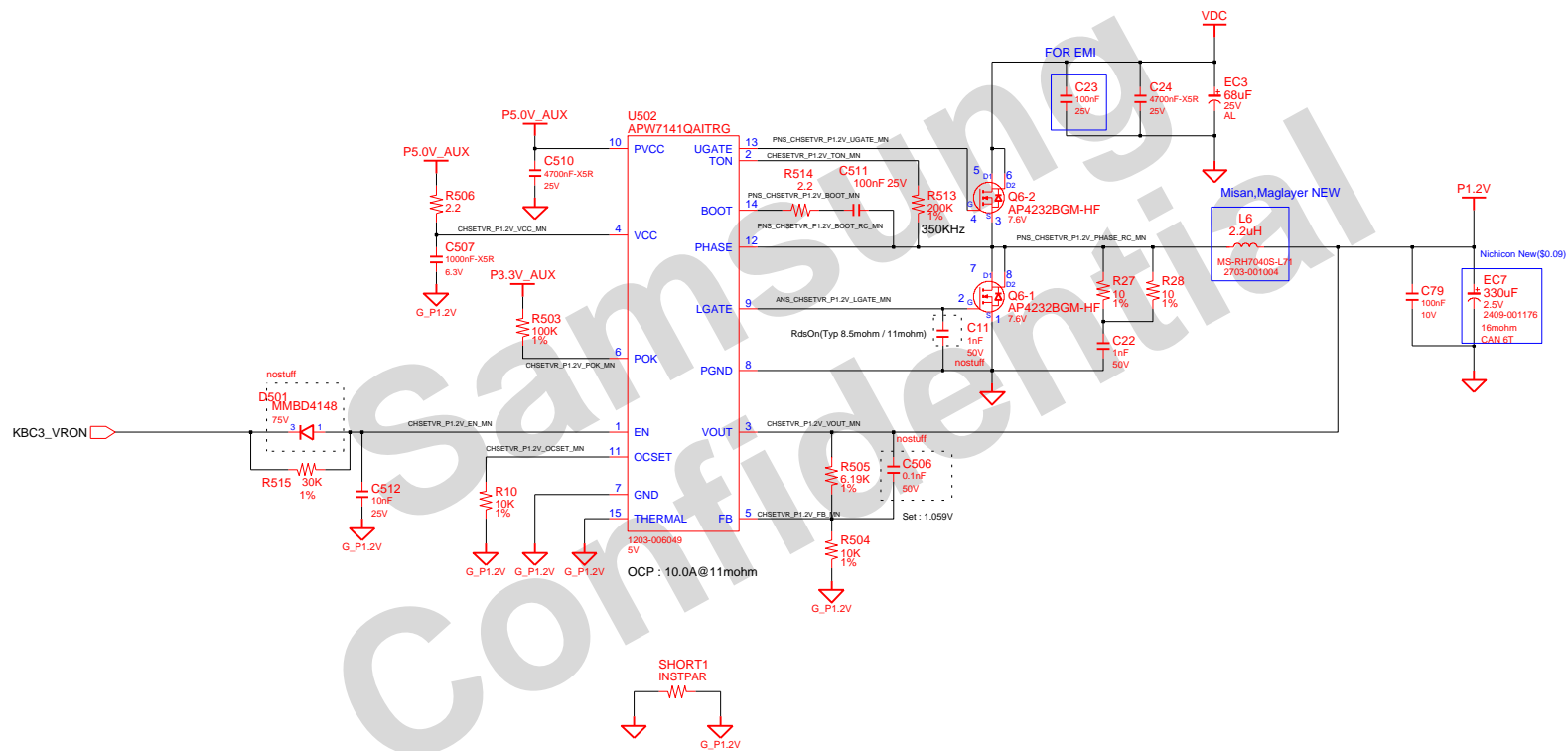
[illegible]

DESIGN	H. J. Rø	DATE	9/3/2009	TITLE Bremen-D PWR MV RX881 P1.1V	SAMSUNG ELECTRONICS
CHECK	K. Y. Kim	DEV. STEP	ADV1		
APPROVAL	H. K. Park	REV	1.1		
MODULE CODE	LAST EDIT		October 10, 2009 16:50:44 PM		

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CHIPSET POWER(P1.2V)



DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1	PWR MV RX881	ELECTRONICS	
APPROVAL	H.K.Park	REV	1.1	P1.2V	PART NO.	BA41-xxxxxA
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	53	OF 61

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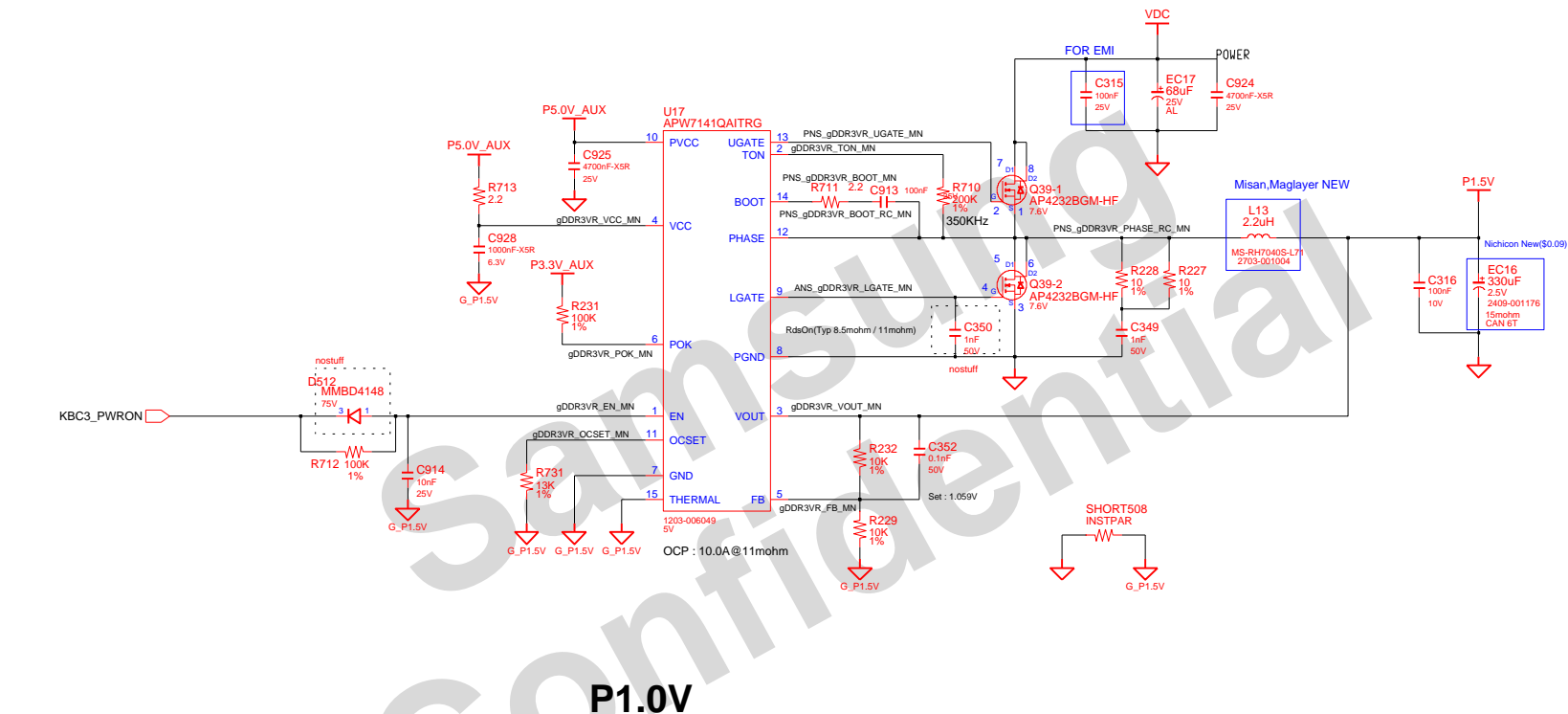
GFX3_VOLTID		
G1	G0	
1	1	0.90V (0.904V)
1	0	0.95V (0.950V)
0	1	1.00V (1.001V)
0	0	1.05V (1.050V)

DRAW	H.J.Ra	DATE	9/23/2008	Bremen-D PWR GFX GFX POWER	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	AD/V1		
APPROVAL	H.K.Park	REV	1.1		
MODULE CODE	LAST EDIT				
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gDDR3 POWER(P1.5V)

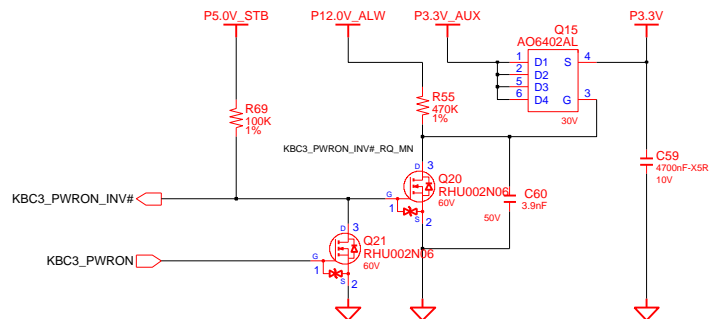


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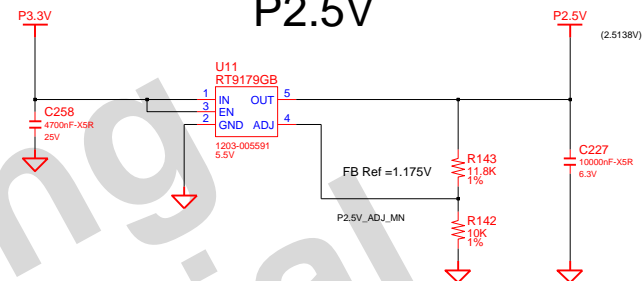
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Switched Power

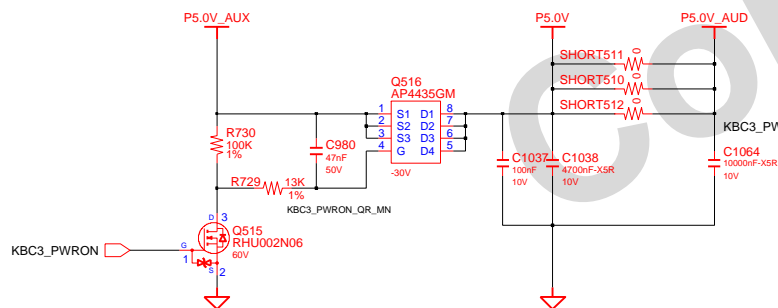
Switched Power On (P3.3V)



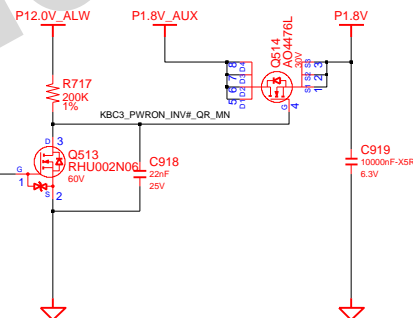
P2.5V



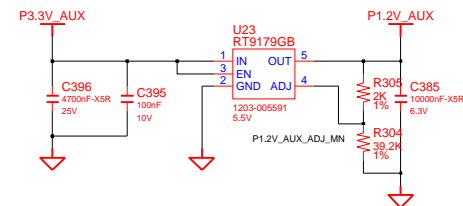
Switched Power On (P5.0V)



Switched Power On (P1.8V)



P1.2V_AUX

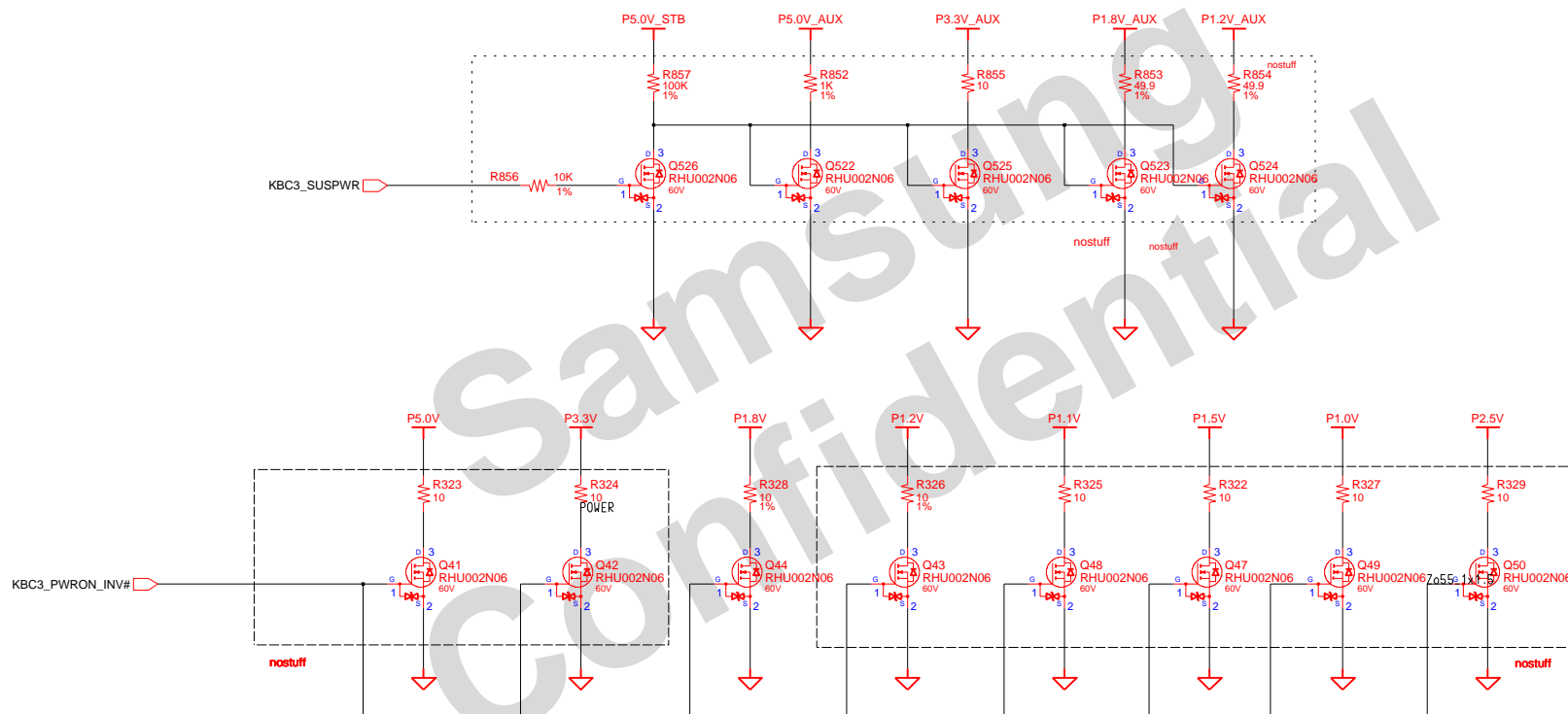


DESIGN	H.J.Ro	DATE	8/22/2009	TITLE	Bremen-D PWR_MV_SWITCHED SWITCHED POWER	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	56 OF 61	

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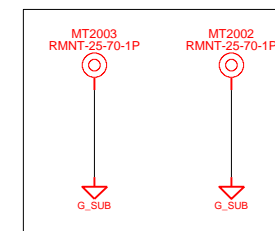
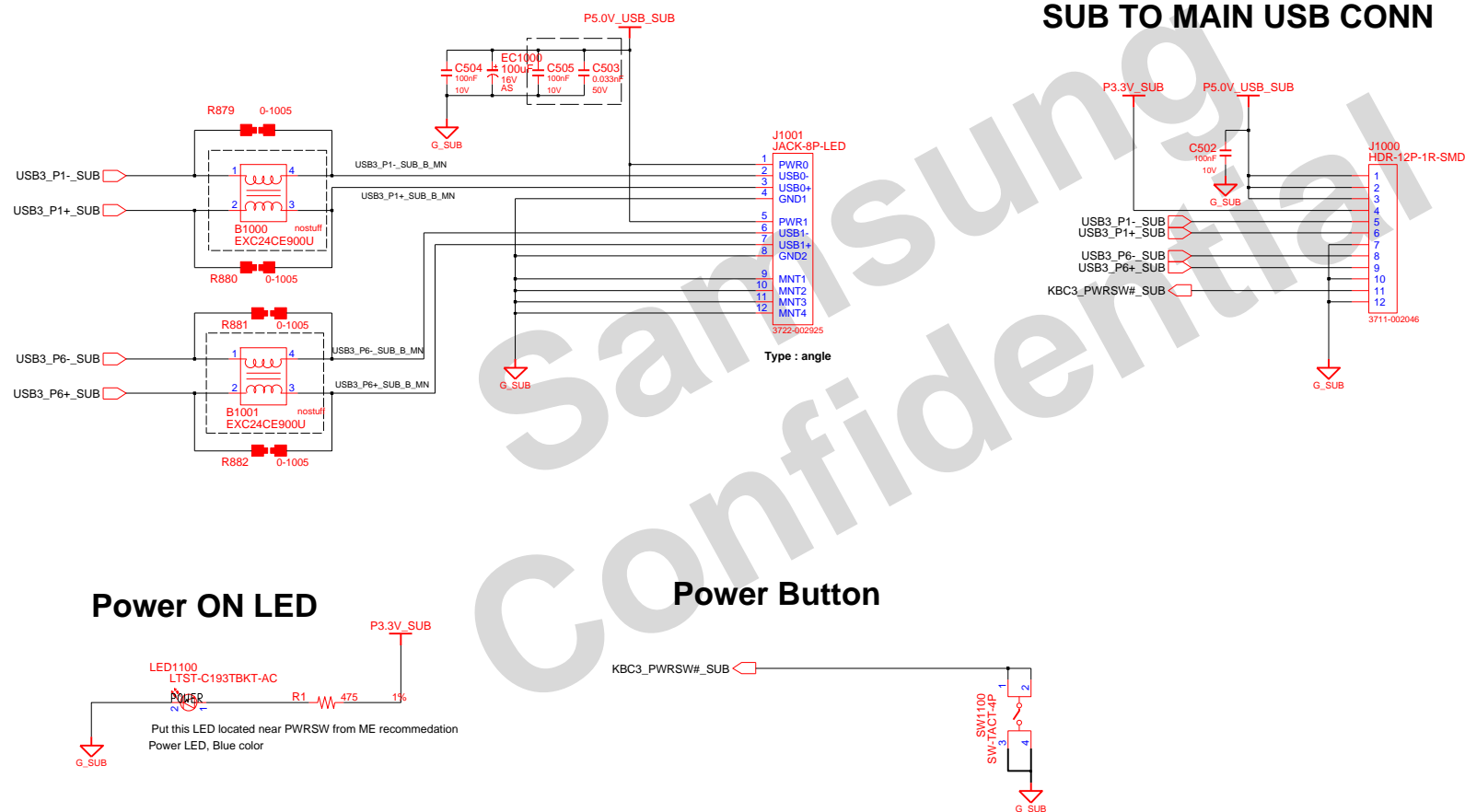
POWER DISCHARGER



DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1		PWR_MV_DISCHARGER	
APPROVAL	H.K.Park	REV	1,1		DISCHARGER LOGIC	
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	57	OF 61

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SUB TO MAIN USB CONN



USB sub board mount hole

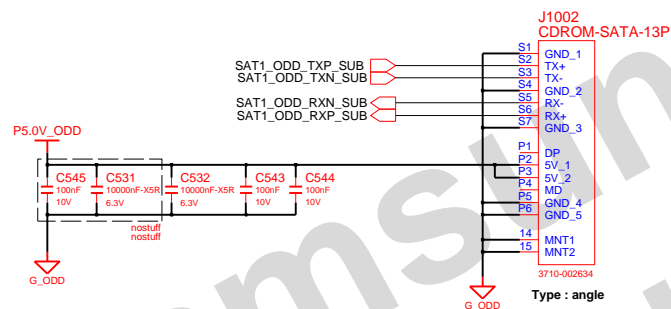
DRAW	H.J.Ra	DATE	9/23/2008	Bremen-D SUB BOARD1 USB PORT, POWER SW SUB BOARD	SAMSUNG ELECTRONICS	
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1		PART NO.	BA41-xxxxxxA
MODULE CODE	LAST EDIT				October 10, 2009 16:50:44 PM	PAGE 58 OF 61

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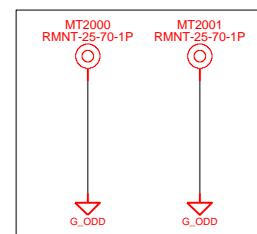
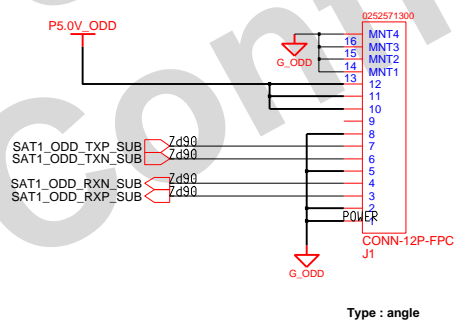
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SATA ODD SUBBOARD

SATA ODD CONN



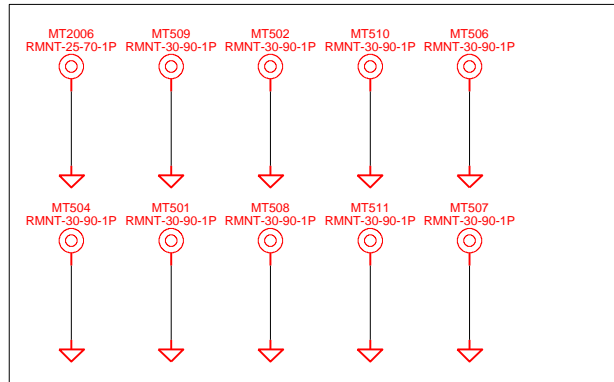
SUB TO MAIN SATA ODD CONN



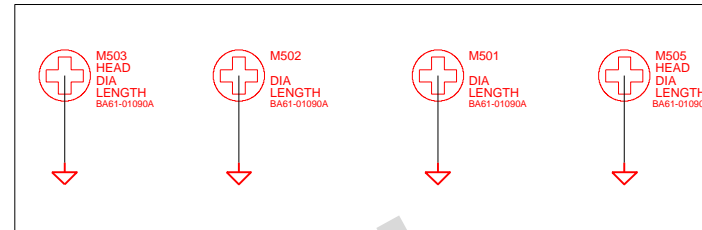
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D SUB BOARD2 SATA ODD SUB BOARD	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	59	OF 61

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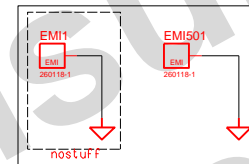
Mainboard Mount



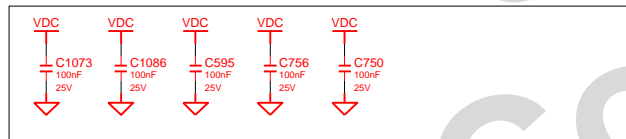
(30,90) x 7, (25,70) x 1



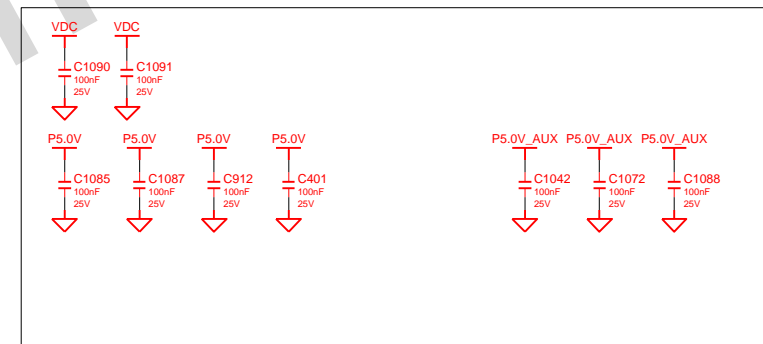
To Support Heatsink



EMI Finger



Add for EMC (Bottom)



Add for EMC (Bottom)

DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D MAIN MOUNT HOLE	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	60	OF 61

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CPU1_LDRTE#
 CPU1_ALL_LDTSTP
 CPU1_LDRSTR#
 CPU1_LDTSTP#
 CPU1_PROCHOT#
 CPU1_PWRGDCPU
 CPU1_SIC
 CPU1_SIO
 CPU1_SVC
 CPU1_SVO
 CPU1_THERMTRIP#
 CPU1_VDDIO_FB
 CPU1_VDDIO_FB#
 CPU1_VDDNB_FB
 CPU1_VDDNB_FB#
 CPU1_VDD_FB
 CPU1_VDD_FB#
 CPU1_VTTENSE#
 CPUPWR_COMP_0_MN
 CPUPWR_COMP_NB_MN
 CPUPWR_ENABLE_MN
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 CPUPWR_FB_NB_MN
 CPUPWR_FSET_NB_MN
 CPUPWR_ISET_0_MN
 CPUPWR_OCSET_MN
 CPUPWR_OFS_VFIXEN_MN
 CPUPWR_RBIAS_MN
 CPUPWR_RIM_MN
 CPUPWR_TDIFF_0
 CPUPWR_VIN_MN
 CPUPWR_VSEN1_MN
 CPUPWR_VW0_MN
 CPU_DEREG_0_R_MN
 CPU_VDDA1_B_MN
 CRT3_BLUE
 CRT3_BLUE_L_MN
 CRT3_DDCCLK
 CRT3_DDCDATA
 CRT3_GREEN
 CRT3_GREEN_L_MN
 CRT3_HSYNC
 CRT3_0V_D_MN
 CRT3_RED
 CRT3_RED_L_MN
 CRT3_VSYNC
 CRT3_DDCCLK
 CRT3_DDCDATA
 CRT3_DDCDATA_CLK_D_MN
 CRT3_HSYNC_R_MN
 CRT3_HSYNC_R_PSN_MN
 DDR3V3R_KBC3_PWRON_0V_75V_RQ0_MN
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 DDR3V3R_PGOOD_MN
 DDR3V3R_TRIP_MN
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 FAN3_FDBACK#
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 GDDR3V3R_EN_MN
 GDDR3V3R_FB_MN
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 GDDR3V3R_POK_MN
 GDDR3V3R_TON_MN
 GDDR3V3R_TOK_MN
 L03_EDIO_CLK

G0DR3VR_VCC.MN
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 G0FX1.MVREFSA.MN
 G0FX3.GPI02
 G0FX3.VOLTID0
 G0FX3.VOLTID1
 G0FX3.VOLTID2
 G0FX.AVDD_0.B.N
 G0FX.CLKTESTA_C.R.MN
 G0FX.DPA.VDDI0_0.R.MN
 G0FX.DPA.VDDI0_1.R.MN
 G0FX.DPCD.CALR_0.R.MN
 G0FX.DPEF.CALR_0.R.MN
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 G0FX.DPE.VDDI0_1.B.N
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 G0FX.DPLL.VDDC_0.B.N
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 G0FX.DVPDATA_21.R.MN
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 G0FX.MPV18_2.B.N
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 KBC3_SMDATA#
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 KBC3_SPT_CSO#
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 KBC3_SPT_DO#
 KBC3_SPMUTE#
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 MEMO_SAT_R_M_N
 MEMO_CALRN1#
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 NB_TESTMODE_R_M_N
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 NB_VDDA18_P_R_M_N
 P2_5V_ADJ#

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 PC3_3V_VDD_INV_EN_Q.MN
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 PEG3_HDMI_DATA
 PEG3_HPD_HPMI
 PEG3_LCDVDOWN
 PEG5_SV_POWER_D.MN
 PEG5_HDMI_CLK
 PEG5_HDMI_DATA
 PEG5_HOT_PLUG_DETECT_R.MN
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 PEX3_RST#
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 PMS_PCIE_CALIP_R.MN
 PMS_PCIE_PVID_B.MN
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 PMS_SYSVR_TG2_MN
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00SP13_CS0
00SP13_MISO
00SP13_MOSI
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00SYSVR_ENTRIP2_MN
00SYSVR_FB1_MN
00SYSVR_FB2_MN
00SYSVR_T0PSEL_MN
00SYSVR_T0NSEL_MN
00SYSVR_VIN_MN
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00TH_VDD_3V_R_MN
00TP5E_BUTTON#
00TP5R_BUTTON#
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01_8V_VDD01
01BGA1E
01BGA1E
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01CPU_CORE
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01C_AUD
01C_AUD
01C_CHG
01C_CHG
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01VCC_ADPT
01VCC_ADPT
01VCC_CHG
01VCC_CHG
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01VDD_CPU_NB
01C_CPU
01C_CPU
01C_DDR
01C_DDR
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01C_P1_2V
01C_P1_2V
01C_P1_5V
01C_P1_5V
01C_P3_3V
01C_P3_3V
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01PG_9V_AUX
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01P1_2V
01P1_2V_AUX
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01P3_V2VDD
01P3_V2VDD
01P3_V2VDD

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- ☐ OP3.3V_AUX
- ☐ OP3.3V_LED
- ☐ OP3.3V_LED
- ☐ OP3.3V_MCD
- ☐ OP3.3V_MCD
- ☐ OP3.3V_MICOM
- ☐ OP3.3V_MICOM
- ☐ OP4.75V_AUD
- ☐ OP4.75V_AUD
- ☐ OP5.0V_AUD
- ☐ OP5.0V_AUD
- ☐ OP5.0V_AUX
- ☐ OP5.0V_AUX
- ☐ OP5.0V_STB
- ☐ OP5.0V_STB
- ☐ PRIC_BAT
- ☐ VCC_CRT
- ☐ VDD_LED